NEW DATA UPDATE 5

NATIONAL SEMICONDUCTOR CORPORATION

DECEMBER 1981

NEW DATA UPDATE 5

NATIONAL SEMICONDUCTOR CORPORATION

The New Data Update 5 is provided by National Semiconductor in order to keep you abreast of the latest products available. This special issue features the first pages of data sheets published July through December 1981 (2 quarters). Two alphanumerical indexes, one by device number and one by device function, serve as guides to the contents of this Update (these indexes/tables of contents are located in the front of the book). Two additional indexes serve as ordering guides for datasheets printed in 1981 and all applications notes and briefs which are still available (these indexes are located in the back of the book).

Circle the appropriate update number on the business reply card (centerfold), add postage, and drop it in the mail to receive the complete data sheet of your choice. Many datasheets in the same product group will have identical update numbers and will be sent as a package. To order publications without an update number, please use the order number provided in the index and write it in one of the blanks provided on the reply card. Due to the costs of handling and mailing, we ask that you limit your requests to no more than 5 items.

To purchase any of the Data Bookshelf volumes, please use the order form immediately following the Data Bookshelf listings in the back of the book.

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National Semiconductor

November 1981

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters which use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

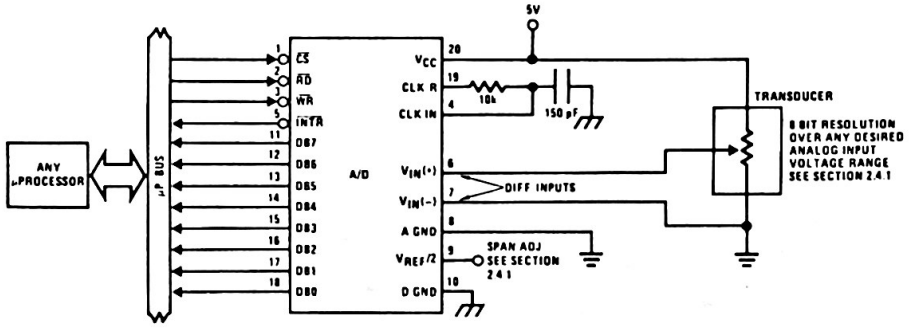
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed — access time — 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

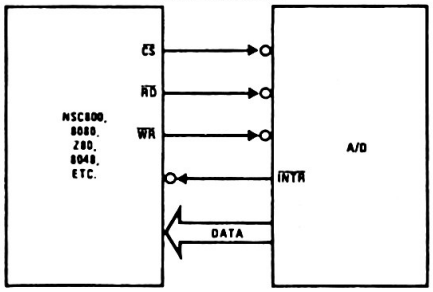
Key Specifications

- Resolution — 8 bits
- Total error — ±1/4 LSB, ±1/2 LSB and ±1 LSB
- Conversion time — 100 μs

Typical Applications



8080 Interface



ERROR SPECIFICATION (INCLUDES FULL SCALE, ZERO ERROR, AND NON LINEARITY)			
PART NUMBER	FULL SCALE ADJUSTED	$V_{REF}/2$ = 2.500 V_{DC} (NO ADJUSTMENTS)	$V_{REF}/2$ = NO CONNECTION (NO ADJUSTMENTS)
ADC0801	±1/4 LSB	±1/2 LSB	
ADC0802			
ADC0803	±1/2 LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

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ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

National Semiconductor

November 1981
PRELIMINARY

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single ended or differential inputs and channel assigned by a 4-bit serial word at the serial I/O.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8-bits of resolution.

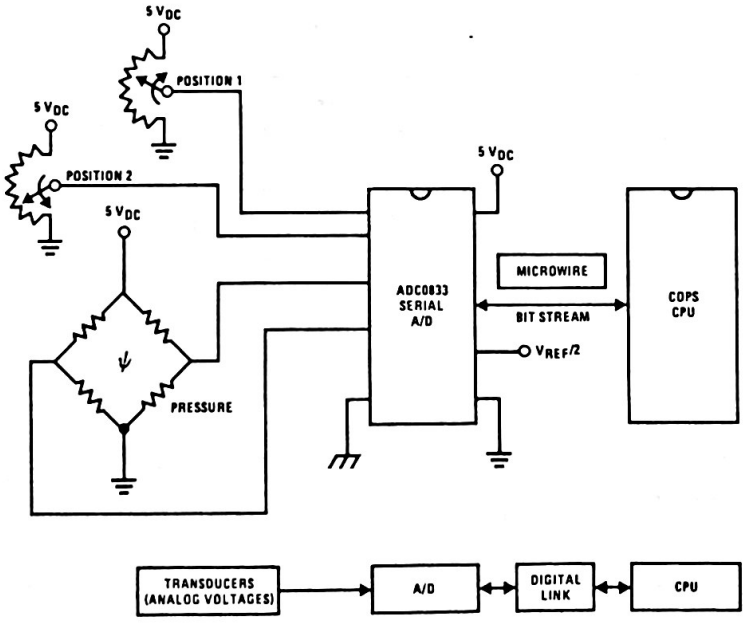
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to 8048, 8049 or 8050
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3" standard width 14-pin DIP package

Key Specifications

■ Resolution	8-Bits
■ Total Unadjusted Error	± 1/2 LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	80 μs

Typical Application



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National Semiconductor

November 1981
PRELIMINARY

ADC1001, ADC1021 10-Bit μP Compatible A/D Converters

General Description

The ADC1001 and ADC1021 are CMOS, 10-bit successive approximation A/D converters. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

The 24-pin ADC1021 outputs 10 bits in parallel and is intended for interface to a 16-bit data bus.

A differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 10 bits of resolution.

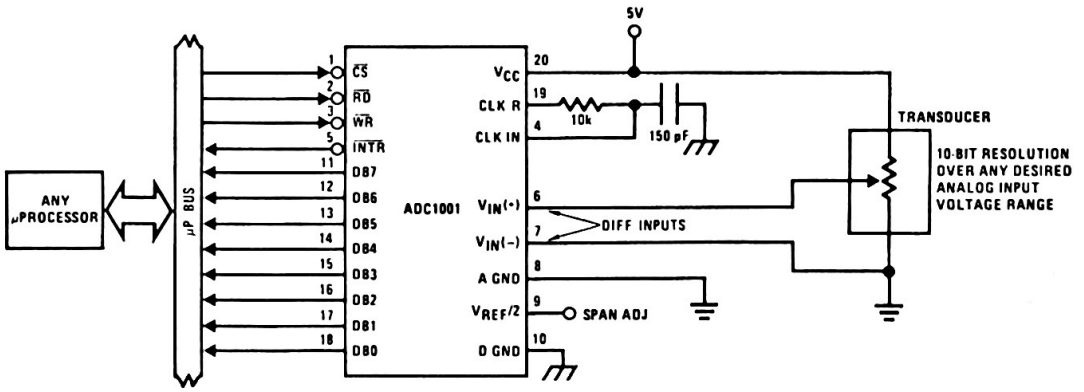
Features

- ADC1001 is pin compatible with ADC0801 series 8-bit A/D
- Compatible with NSC800 and 8080 μP derivatives — no interfacing logic needed — access time 170 ns
- Easily interfaced to 6800 μP derivatives with minimal external logic
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3" standard width 20-pin DIP package or 24 pins with 10-bit parallel output

Key Specifications

■ Resolution	10 bits
■ Linearity error	± 1/2 LSB and ± 1 LSB
■ Conversion time	200 μs

Typical Application



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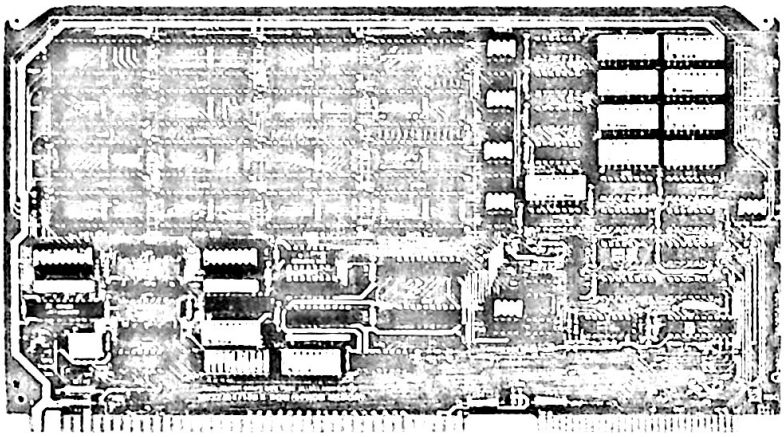
BLC-464
128K PROM/ROM Expansion Board



- **16K to 128K Capacity Compatible With Seven PROM (ROM) Device Types: 2758, 2716 (2316), 2732 (2332), or 2764 (37000)**
- **Single 5V Power Supply**
- **Plugs Into Standard BLC-604/614 Card Cage or Equivalent**
- **Compatible With Industry Standard MULTIBUS™ (IEEE 796)**
- **Address-Assignable Anywhere Within 16M Byte Memory**
- **Switch-Selectable Minimum Access Time From 35 ns to 1435 ns**
- **Operation in 8-Bit or 16-/8-Bit Mode**
- **Plug Replacement for SBC-464, With Doubled Capacity**

Product Overview

The BLC-464 PROM/ROM Expansion Board provides a highly flexible, low cost, read-only memory expansion board compatible with any Series/80 Board Level Computer through the standard MULTIBUS interface. The fully expanded board accomodates 16 PROM/ROM devices for capacities of 16K, 32K, 64K, or 128K bytes. Compatible PROM/ROMs are the 2758 (1K x 8), 2716/2316 (2K x 8), 2732/2332 (4K x 8), and 2764/37000 (8K x 8). The BLC-464 requires only a $+5V_{DC}$ power supply.

Functional Description

The BLC-464 decodes a memory address received on the MULTIBUS address lines and gates buffered memory data back to the bus. The user selects memory size, memory organization, base addresses, and board access time with on-board DIP switches, option blocks, and Berg jumpers.

In a general read operation, a bus master puts a memory address on the MULTIBUS address lines. The BLC-464 base address select circuitry and chapter/page select circuitry decode the incoming information to determine whether the BLC-464 is being addressed. If so, appropriate information is sent to the control logic and chip select circuitry, and RAM is inhibited in case of address overlap. In response to a bus master memory read command, the BLC-464 starts an access time counter, the addressed PROM/ROM devices are selected, and data is transferred to the MULTIBUS data lines via the memory buffer. When the board access time has elapsed, the BLC-464 informs the bus master that memory data is available on the bus. The bus master then accepts the data and issues a signal ending the read operation.

Circle DATA UPDATE No. 950501

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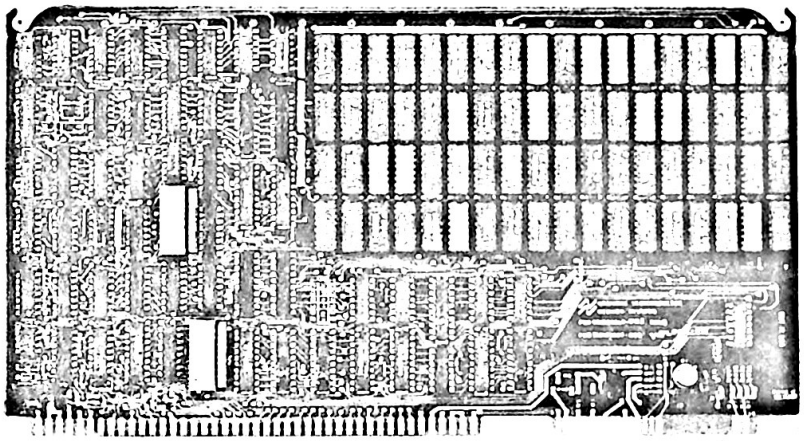
National Semiconductor

PRELIMINARY
September 1981

BLC-0128
128K-Byte Memory Card



- **Features**
  - Parity (error detection)
  - Selectable parity interrupt
  - 128K bytes memory
- **Enhanced Systems Performance**
  - On-board refresh and control logic
  - Internal (transparent) refresh
  - Optional external refresh
  - Battery backup capability
- **Compatible with all Series/80 Boards and Card Cages**
- **Flexible Systems Capability**
  - 8- or 16-bit data bus
  - 20- or 24-bit memory addressing
  - 8- or 16-bit I/O addressing
- **Ease of Maintenance**
  - Control status register logs failures for CPU
  - All RAMs socketed

Product Overview

The BLC-0128 RAM memory cards are designed and tested to provide the users increasing memory requirements while maintaining high level data integrity. The optional parity feature provides the means to verify whether the data is correct.

Parity is a method to detect errors which may occur while reading data from the RAM. In the event a data error occurs the CPU is notified. Error information is also logged in the Control Status Register (CSR). Selectable parity interrupts allow the user to determine which interrupt request line is used. Any one of eight interrupt request lines may be selected.

Functional Description

The BLC-0128 is a 128K byte (128K × 8,9) random access memory card designed to be compatible with all Series/80 microcomputers. Utilizing the available options, the BLC-0128 is operational in a wide variety of configurations including 8- or 16-bit I/O addressing. Set via a DIP switch, the starting address may be set on any 16K word boundary within the 16M byte range.

Control Status Register

Parity error information is stored into an on-board CSR. The CSR is a software addressable 16-bit Control Status Register. The CSR may be set to respond

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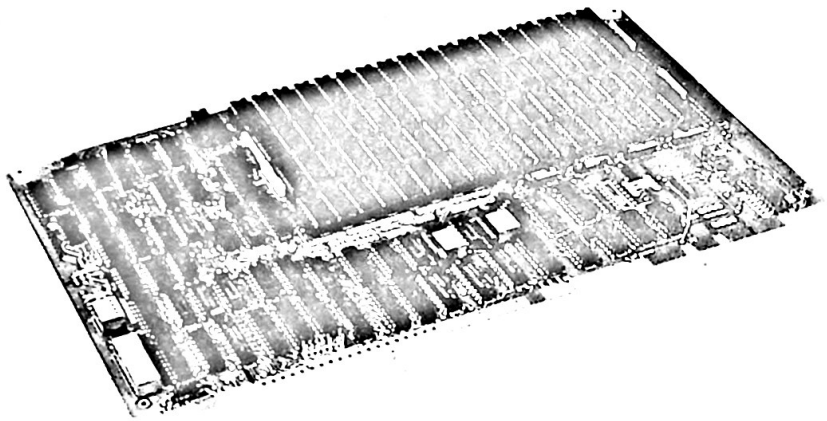
BLC-0512
512K-Byte Memory Card Family



- **Features**
  - Parity (error detection)
  - Selectable parity interrupt
  - 512K bytes memory
- **Enhanced Systems Performance**
  - On-board refresh and control logic
  - Internal (transparent) refresh
  - Optional external refresh
  - Battery backup capability
- **MULTIBUS™ IEEE 796 Standard**
- **Compatible with all Series/80 Boards and Card Cages**
- **Flexible Systems Capability**
  - 8- or 16-bit data bus
  - 20- or 24-bit memory addressing
  - 8-, 12-, or 16-bit I/O addressing
- **Ease of Maintenance**
  - Control status register logs failures for CPU
  - All RAMs socketed

Product Overview

The BLC-0512 RAM memory cards are designed and tested to meet the users increasing memory requirements while maintaining a high level of data integrity. The card is available in 128, 256, 384 and 512K bytes of memory. The optional parity feature enhances data integrity.

Parity is a method to detect errors which may occur while reading data from the RAM. In the event a data error occurs the CPU is notified. Error information is also logged in the Control Status Register (CSR). Selectable parity interrupts allow the user to determine which interrupt request line is used. Any one of eight interrupt request lines may be selected.

Functional Description

The BLC-0512 is a 512K byte (512K × 8,9) random access memory card designed to be compatible with all Series/80 microcomputers. Utilizing the available options, the BLC-0512 is operational in a wide variety of configurations including 8-, 12-, or 16-bit I/O addressing. Set via a DIP switch, the starting address may be set on any 16K word boundary within the 16M byte range.

Control Status Register

Parity error information is stored into an on-board CSR. The CSR is a software addressable 16-bit Control Status Register. The CSR may be set to respond

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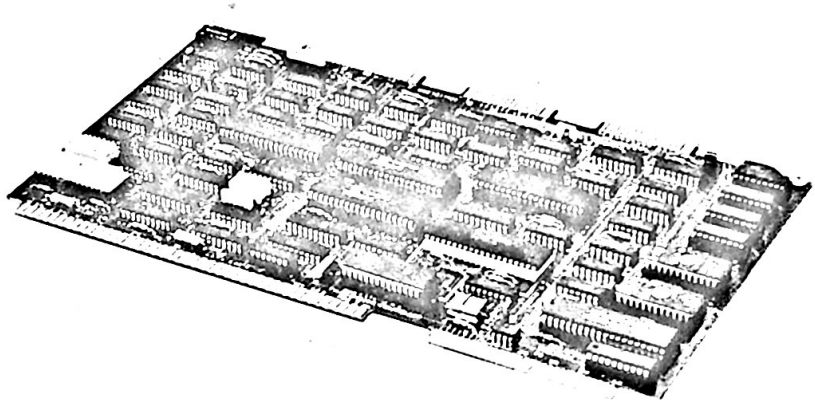
BLC-8224 Double Density Floppy Disk Controller



- **Intelligent Double Density Controller on a Single Series/80 Board**
- **Design Flexibility**
  - Read/Write in IBM System 34 double density (MFM) or IBM 3740 single density (FM) mode
  - FM/MFM selection under program control
  - User definable sector size
  - Switch selectable base addresses allow multiple controller systems
- **24 System Address Lines Providing a 16 Megabyte Address Space**
- **Controls Up to Four Dual or Single Sided, Standard or Mini Drives**
- **CRC Error Checking with Programmed Re-try**
- **Compatible with Popular Model Shugart Diskette Drives**
- **Bus Transfer Rates Up to 1.3M Bits/Second**

Product Overview

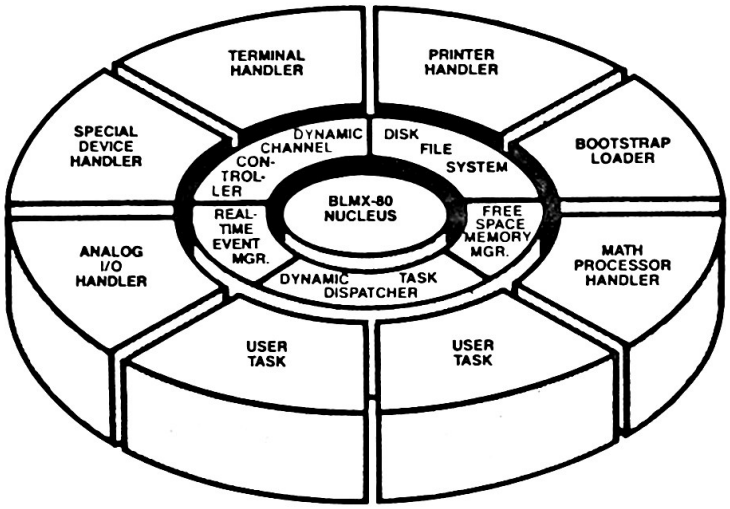
The BLC-8224 Double Density Floppy Disk Controller is a member of National's Series/80 family of intelligent peripheral device controllers. The controller is Multibus™ compatible and provides the Series/80 single board computer user with an easy to use, high performance bulk storage interface. The BLC-8224 uses numerous LSI components, resulting in a powerful single board controller which is economical in terms of space and power consumption, as well as price. Numerous user selectable options are designed in, making the controller highly flexible and easy to use in a wide range of applications requiring large amounts of non-volatile storage.

The BLC-8224 provides a simple upgrade path for current users of the BLC-8221 and BLC-8222 Floppy Disk Controllers. The change is simply in the software to allow for the extra byte for the extended addressing range of the BLC-8224. This extension provides an additional eight bits of address (up to 16 megabytes), thus making the BLC-8224 suitable for applications based on 16-bit CPUs.

Functional Description

The BLC-8224 interfaces to the system bus via I/O, DMA, and Interrupts. The I/O interface is used to pass information from the system CPU to the

BLMX-80
Board-Level, Multitasking Executive



- **Configurability**
  - Fully user configurable
  - Menu selection procedure
  - Hardware independent
- **Compatibility**
  - 8080/8085, Z80®, NSC800
  - Bus-like structure
- **Reliability**
  - Small, efficient nucleus
  - Simple user interface
  - Standard data structures
- **User-Oriented Support**
  - Extensive I/O handlers
  - Analog handlers
  - Disk file system
- **Easy-to-Use**
  - Prompting menus guide system configuration
  - Comprehensible system functions
  - Functional similarity for internal & external calls
  - Re-configurable

Product Overview

The BLMX-80 software system is a real-time, multitasking executive, specifically designed for use with National Semiconductor Corporation's Board Level Computer (BLC) products. It has been optimized for real-time applications such as process control, manufacturing monitoring, and data acquisition systems. The BLMX-80 executive is fully modular and can readily be configured to suit applications needs. It is completely hardware and location independent, thereby providing a fundamental base upon which users can build a wide range of application systems. In addition, BLMX-80 provides a bus-like structure which helps to integrate software with its underlaying hardware through predefined data structures and interconnect procedures. This concept of software-bus architecture insures maximum quality of standardization for compatibility and future expandibility.

The BLMX-80 nucleus requires only 512 bytes of RAM and 2K bytes of ROM. The system contains all major real-time functions including task scheduling, intertask communication and synchronization, interrupt handling and I/O control, as well as many optional features.

The Series/80 CPU boards supported by BLMX-80 include: BLC-80/05, BLC-80/10, BLC-80/11, BLC-80/12, BLC-80/14, BLC-80/11A, BLC-80/12A, BLC-80/14A, BLC-80/116, BLC-80/204, BLC-80/316, and BLC-8715. Support is guaranteed for all future CPU boards with an 8-bit microprocessor.

The peripheral I/O devices and controllers supported by BLMX-80 include: RS232 terminal, teletype terminal, Centronics printer, BLC-711, BLC-724, BLC-732, and BLC-8737 analog I/O boards, and more.

 In-System Emulator is a trademark of National Semiconductor Corp. AG-B30M81/Printed in U S A

National Semiconductor

ADVANCE INFORMATION
JULY 1981

COP410C/COP411C and COP310C/COP311C Fully Static, Single-Chip CMOS Microcontrollers

COP410C/COP411C and COP310C/COP311C
Fully Static, Single-Chip CMOS Microcontrollers

General Description

The COP410C, COP411C, COP310C, and COP311C fully static, single-chip CMOS microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon gate complementary MOS technology. These microcontrollers are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of output configuration options, with an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and BCD data manipulation. The COP411C is identical to the COP410C but with 16 I/O lines instead of 19. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end product cost.

The COP310C/COP311C are exact functional equivalents, but extended temperature range versions of the COP410C/COP411C.

Features

- Lowest power dissipation (40 μW typical)
- Low cost
- Power saving HALT mode with Continue function
- Powerful instruction set
- 512 × 8 ROM, 32 × 4 RAM
- 19 I/O lines (COP410C)
- Two-level subroutine stack
- DC to 4 μs instruction time
- Single supply operation (2.4V to 5.5V)
- General purpose and TRI-STATE® outputs
- Internal binary counter register with serial I/O capability
- LSTTL/CMOS compatible in and out
- Software/hardware compatible with other members of the COP400 family
- MICROWIRE™ compatible serial I/O
- Extended temperature range device available (−40°C to +85°C)

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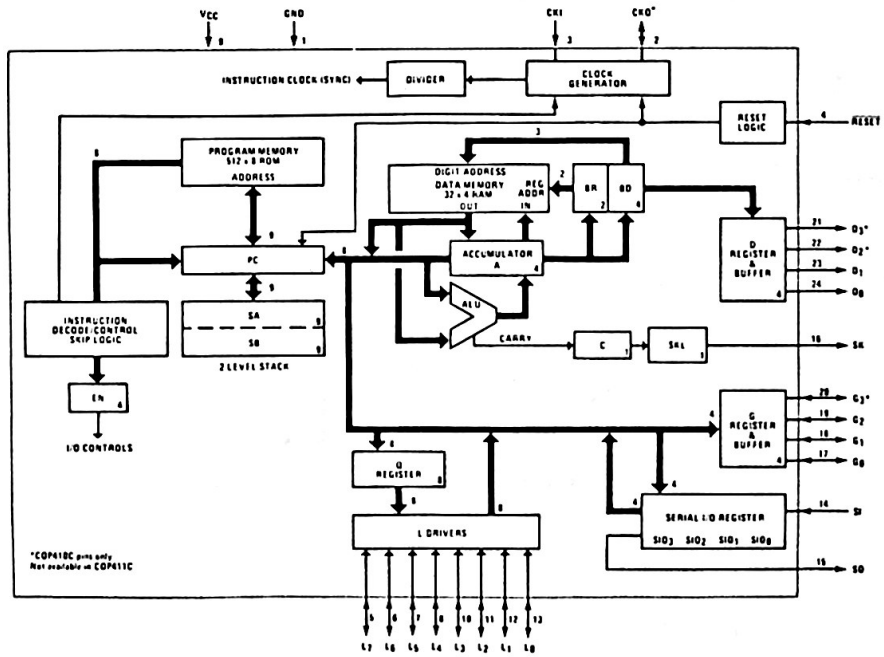

Figure 1. COP410C/COP411C Block Diagram

DA-B25K71/Printed in U.S.A.

National Semiconductor

SEPTEMBER 1981

COP410L/COP411L and COP310L/COP311L Single-Chip N-Channel Microcontrollers

General Description

The COP410L and COP411L Single-Chip N-Channel Microcontrollers are members of the COPS™ family, fabricated using N-channel, silicon gate MOS technology. These Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP411L is identical to the COP410L, but with 16 I/O lines instead of 19. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

The COP310L and COP311L are exact functional equivalents but extended temperature versions of COP410L and COP411L respectively.
The COP401L may be used for exact emulation.

Features

- Low cost
- Powerful instruction set
- 512 x 8 ROM, 32 x 4 RAM
- 19 I/O lines (COP410L)
- Two-level subroutine stack
- 16μs instruction time
- Single supply operation (4.5-6.3V)
- Low current drain (6mA max.)
- Internal binary counter register with MICROWIRE™ serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible in and out
- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of COP400 family
- Extended temperature range device COP310L/COP311L (−40°C to +85°C)
- Wider supply range (4.5-9.5V) optionally available

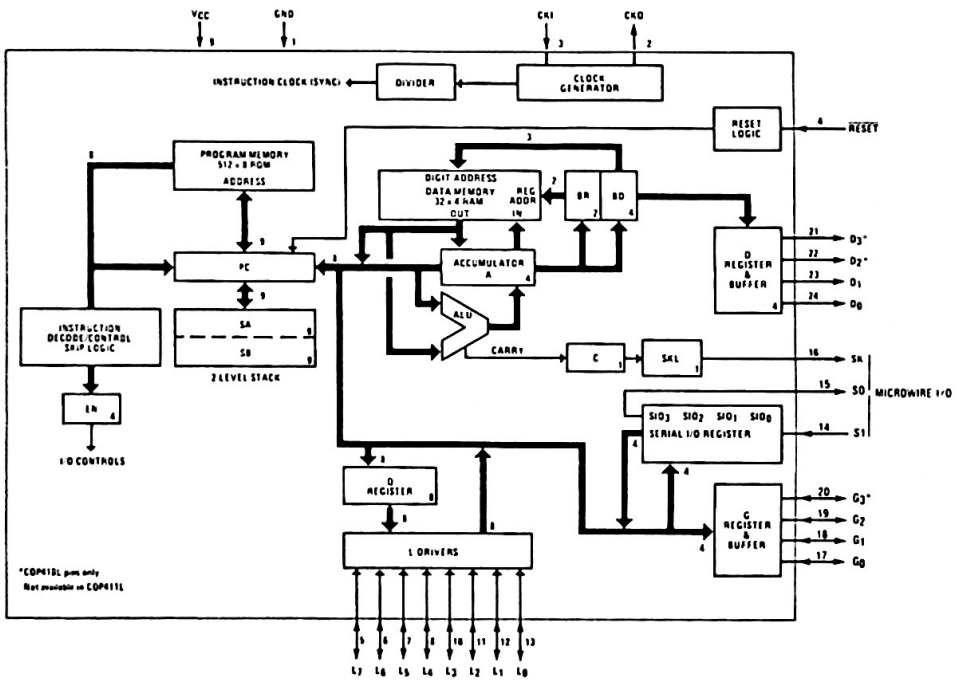

Figure 1. COP410L/411L Block Diagram

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TRI-STATE is a registered trademark of National Semiconductor Corp.

DA-B25M91/Printed in U.S.A.

National Semiconductor

JULY 1981

COP420R/COP444LR Piggyback-EPROM Microcontroller

General Description

The COP420R and COP444LR Piggyback-EPROM microcontrollers are members of the COPS™ family. The COP420R and COP444LR devices are identical to the COP420 and COP444L respectively except that the program ROM has been removed. In place of the ROM each device package incorporates the circuitry and socket to accommodate the Piggyback-EPROM.

The socket provided on the package accepts an MM2716, NMC27C16, MM2758A, or MM2758B EPROM. Each part is a complete microcontroller system with CPU, RAM, I/O, and EPROM socket provided in a single 28-pin package. In a system the COP420R and COP444LR will perform exactly as its mask programmed equivalent.

The complete package allows field test of a system in its final electrical and mechanical configuration. This important benefit facilitates development and debug of a COP400 program prior to masking of a production part.

These devices are also economical in low and medium volume applications or when the program may require changing.

Features

- Exact equivalent of the COP420 and COP444L — plugs into same socket
- Socket and interface for industry standard EPROMs
- Self-contained voltage regulator for EPROM on COP444LR
- Powerful instruction set
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Compatible with all COPS family peripherals
- Internal binary counter register with MICROWIRE™ family peripherals compatible serial I/O
- Software and hardware compatible with other members of the COPS family
- Single supply operation
- Internal presettable time base counter for real time processing
- 4 μs instruction time (COP420R)
- 16 μs instruction time (COP444LR)
- 23 I/O lines

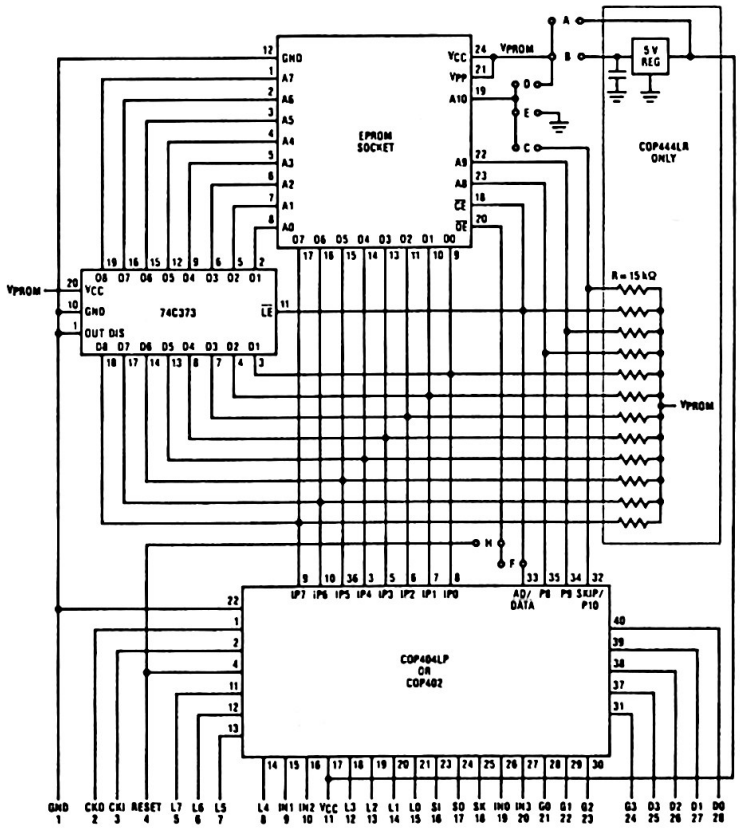

Figure 1. COP420R/COP444LR Block Diagram

DA-B25K71/Printed in U.S.A.

National Semiconductor

SEPTEMBER 1981

COP452/COP453 and COP352/COP353 Frequency Generator and Counter

General Description

The COP452/COP453 and COP352/COP353 are peripheral members of the COPS™ family fabricated using N-channel silicon gate MOS technology. Containing two independent 16-bit counter/register pairs, they are well suited to a wide variety of tasks involving the measurement and/or generation of times and/or frequencies. Included in the features are multiple tone generation, precise duty cycle generation, event counting, waveform measurement, frequency bursts, delays, and "white noise" generation. An on-chip zero crossing detector can trigger a pulse with a programmed delay and duration. The COP453 is identical to the COP452, but operates with supply voltages up to 9.5 volts. The COP352/COP353 are extended temperature versions of the COP452/COP453, respectively. The COP352/COP353 are functional equivalents of the COP452/COP453.

The COP452 series peripheral devices can perform numerous functions that a microcontroller alone cannot perform. They can execute one or more complex tasks, attaining higher accuracies over a broader frequency range than a microcontroller alone. These devices remove repetitive yet demanding counting, timing, and frequency related functions from the microcontroller, thereby freeing it to perform other tasks or allowing the use of a simpler microcontroller in the system.

Features

- Unburdens microcontroller by performing "mundane" tasks
- Wider range and greater accuracy than microcontroller alone
- Generates frequencies, frequency bursts, and complex waveforms
- Measures waveform duty cycle
- Two independent pulse/event counters
- True zero crossing detector triggers output pulse
- White noise generator
- Compatible with all COP400 microcontrollers
- MICROWIRE™ compatible serial I/O
- 14-pin package
- Single supply operation
  (4.5-6.3V, COP452; 4.5-5.5V, COP352)
  (4.5-9.5V, COP453; 4.5-7.5V, COP353)
- Low cost
- Crystal or external clock
  (25 kHz to 4.44 MHz, COP452/COP453)
  (64 kHz to 4.0 MHz, COP352/COP353)
- TTL compatible

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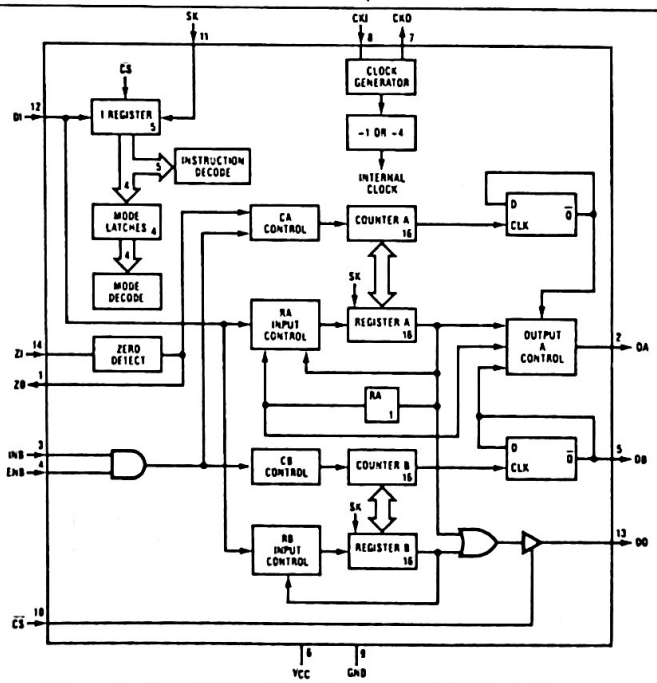

Figure 1. COP452/COP453, COP352/COP353 Block Diagram

DA25M91/Printed in U.S.A.

National Semiconductor

AUGUST 1981

COP472 Liquid Crystal Display Controller

General Description

The COP472 Liquid Crystal Display (LCD) Controller is a peripheral member of the COPS™ family, fabricated using CMOS technology. The COP472 drives a multiplexed liquid crystal display directly. Data is loaded serially and is held in internal latches. The COP472 contains an on-chip oscillator and generates all the multi-level waveforms for backplanes and segment outputs on a triplex display. One COP472 can drive 36 segments multiplexed as 3 x 12 (4½ digit display). Two COP472 devices can be used together to drive 72 segments (3 x 24) which could be an 8½ digit display.

Features

- Direct interface to TRIPLEX LCD
- Low power dissipation (100 μW typ.)
- Low cost
- Compatible with all COP400 processors
- Needs no refresh from processor
- On-chip oscillator and latches
- Expandable to longer displays
- Software compatible with COP470 V.F. Display Driver chip
- Operates from display voltage
- MICROWIRE™ compatible serial I/O
- 20-pin dual-in-line package

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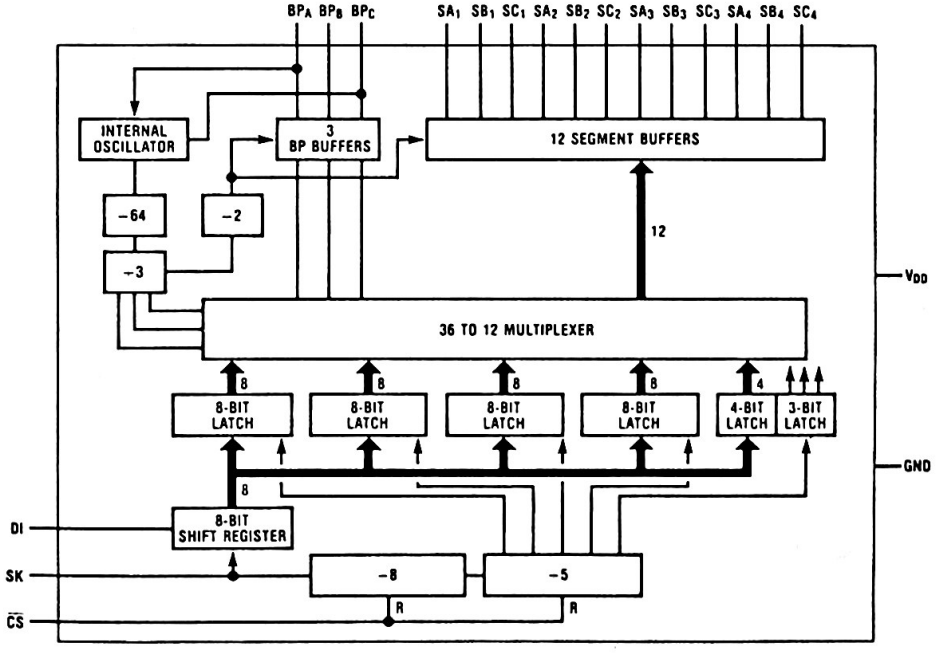

COP472 Block Diagram

DA-B25M81/Printed in U.S.A.

National Semiconductor

JULY 1981

COP498/COP398 Low Power CMOS RAM and Timer (RAT™)
COP499/COP399 Low Power CMOS Memory

General Description

The COP498/398 Low Power CMOS RAM and Timer (RAT) and the COP499/399 Memory are peripheral members of the COPS™ family, fabricated using low power CMOS technology. These devices provide external data storage and/or timing, and are accessed via the simple MICROWIRE™ serial interface. Each device contains 256 bits of read/write memory organized into 4 registers of 64 bits each; each register can be serially loaded or read by a COPS controller.

The COP498/398 also contain a crystal-based timer for timekeeping purposes, and can provide a "wake-up" signal to turn on a COPS controller. Hence, these devices are ideal for applications requiring very low power drain in a standby mode, while maintaining a real-time clock (e.g., electronically-tuned automobile radio). Power is minimized by cycling controller power off for periods of time when no processing is required.

The COP499/399 contain circuitry that enables the user to turn a controller on and off while maintaining the integrity of the memory.

A COP400 series N-channel microcontroller coupled with a COP498 (or 499) RAM/Timer offers a user the low-power advantages of an all CMOS system and the low-cost advantage of an NMOS system. This type of system is ideally suited to a wide variety of automotive and instrumentation applications.

Features

- Low power dissipation
- Quiescent current = 40 nA typical (25°C, V_{CC} = 3.0 V)
- Low cost
- Single supply operation (2.4 V–5.5 V)
- CMOS-compatible I/O
- 4 × 64 serial read/write memory
- Crystal-based selectable timer — 2.097152 MHz or 32.768 kHz (COP498/398)
- Software selectable 1 Hz or 16 Hz "wake-up" signal for COPS controller (COP498/398)
- External override to "wake-up" controller
- Compatible with all COP400 processors (processor $V_{CC} \leq 9.5$ V)
- MICROWIRE-compatible serial I/O
- Memory protection with write enable and write disable instructions
- 14-pin dual-in-line package (COP498/398) or 8-pin dual-in-line package (COP499/399)

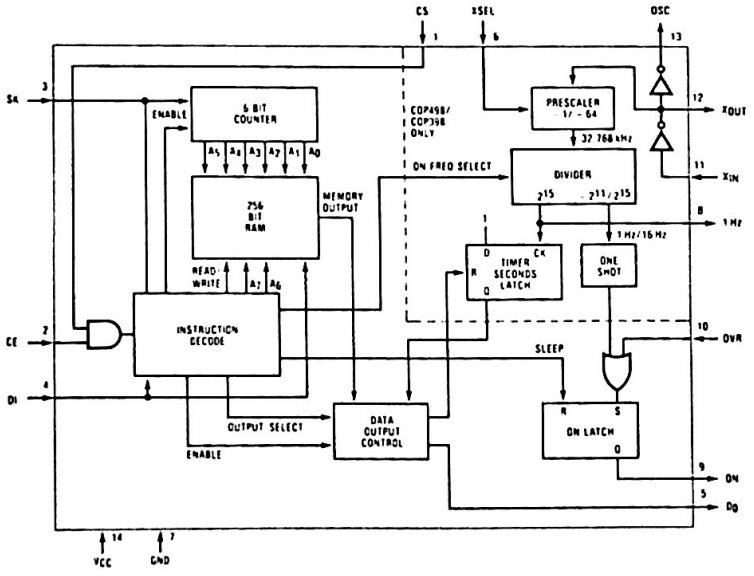

Figure 1. Block Diagram

National Semiconductor

PRELIMINARY INFORMATION
JULY 1981

COP2404 ROMless Dual CPU Microcontroller

General Description

The COP2404 ROMless Dual CPU Microcontroller is a member of the COPS™ family, fabricated using N-channel, silicon gate MOS technology. This microcontroller contains two identical CPUs with all system timing, internal logic, RAM and I/O necessary to implement dedicated control functions in a variety of applications, and is identical to a COP2440 device, except that the ROM has been removed; pins have been added to output the ROM address and to input ROM data. In a system, the COP2404 will perform exactly as the COP2440; this important benefit facilitates development and debug of a COP2440 program prior to masking the final part. Features include single supply operation, various output configurations, and an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output and data manipulation. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a dual CPU microcontroller at a low end-product cost.

These microcontrollers are appropriate choices in many demanding control environments, especially those with human interface. Further, the high throughput and MICROBUS™ I/O facilitate numerous machine interface applications. The two CPUs provide on one chip the ability to handle two simultaneous but totally independent real time events.

Features

- Exact circuit equivalent of COP2440
- Standard 48-pin dual-in-line package
- Interfaces with standard PROM or ROM
- Two independent processors
- Dual CPU simplifies task partitioning — easy to program
- Enhanced, more powerful instruction set
- 160 × 4 RAM, addresses up to 2k × 8 ROM
- MICROBUS compatible
- Zero-crossing detect circuitry
- True multi-vectored interrupt from 4 selectable sources (plus restart)
- Four-level subroutine stack for each processor (in RAM)
- 4 μs execution time per processor (non-overlapping)
- Single supply operation (4.5V-6.3V)
- Programmable time-base counter for real-time processing
- Internal binary counter/register with MICROWIRE™ compatible serial I/O
- General purpose and TRI-STATE® outputs
- TTL/CMOS compatible in and out
- Software/hardware compatible with other members of COP400 family
- Compatible single-processor device available

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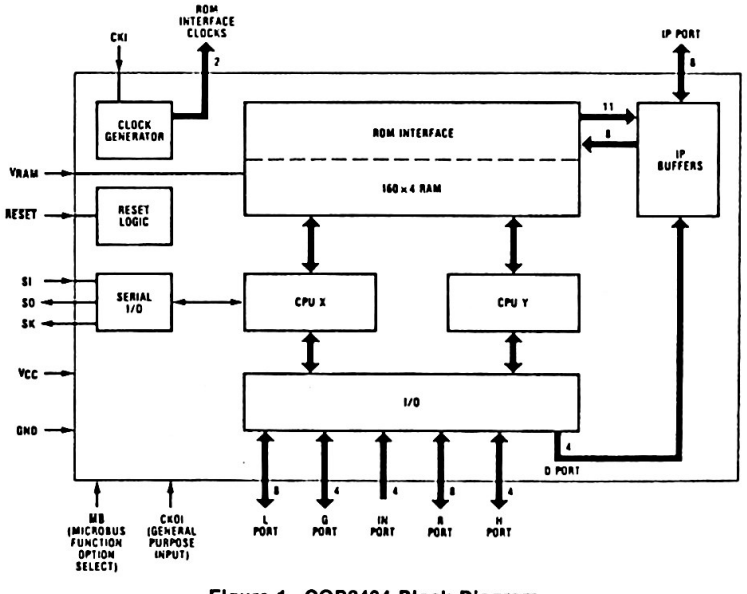

Figure 1. COP2404 Block Diagram

DA-B25K71/Printed in U.S.A.

National Semiconductor

AUGUST 1981

COP2440/COP2441/COP2442 and COP2340/COP2341/COP2342 Single-Chip Dual CPU Microcontrollers

General Description

The COP2440, COP2441, COP2442, COP2340, COP2341, and COP2342 Single-Chip Dual CPU Microcontrollers are members of the COPS™ family, fabricated using N-channel, silicon gate MOS technology. These microcontrollers contain two identical CPUs with all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, various output configuration options, and an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and data manipulation. The COP2440 is a 40-pin chip and the COP2441 is a 28-pin version of the same circuit (12 I/O lines removed). The COP2442 is a 24-pin version (4 more input lines removed). The COP2340, COP2341, COP2342 are functional equivalents of the above devices respectively, but operate with an extended temperature range (−40°C to +85°C). Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized dual CPU microcontroller at a low end-product cost.

These microcontrollers are appropriate choices in many demanding control environments, especially those with human interface. Further, the high throughput and MICROBUS™ I/O facilitate numerous machine interface applications. The two CPUs provide the ability to handle two simultaneous but totally independent real time events on one chip.

Features

- Two independent processors
- Dual CPU simplifies task partitioning—easy to program
- Enhanced, more powerful instruction set
- 2k × 8 ROM, 160 × 4 RAM
- 35 I/O lines (COP2440)
- Zero-crossing detect circuitry with hysteresis
- True multi-vectored interrupt from 4 selectable sources (plus restart)
- Four-level subroutine stack for each processor (in RAM)
- 4 μs execution time per processor (non-overlapping)
- Single supply operation (4.5V–6.3V)
- Programmable time-base counter for real-time processing
- Internal binary counter/register with MICROWIRE™-compatible serial I/O
- General purpose and TRI-STATE® outputs
- TTL/CMOS-compatible in and out
- LED drive capability
- MICROBUS-compatible
- Software/hardware compatible with other members of the COP400 family
- Extended temperature range devices COP2340, COP2341, COP2342 (−40°C to +85°C)
- Compatible single-processor device available (COP440 series)

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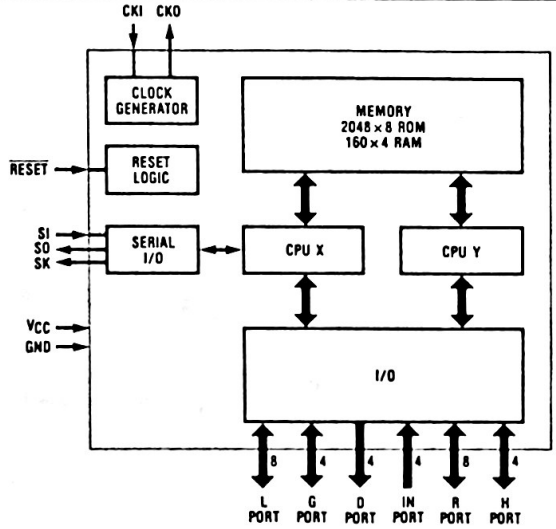


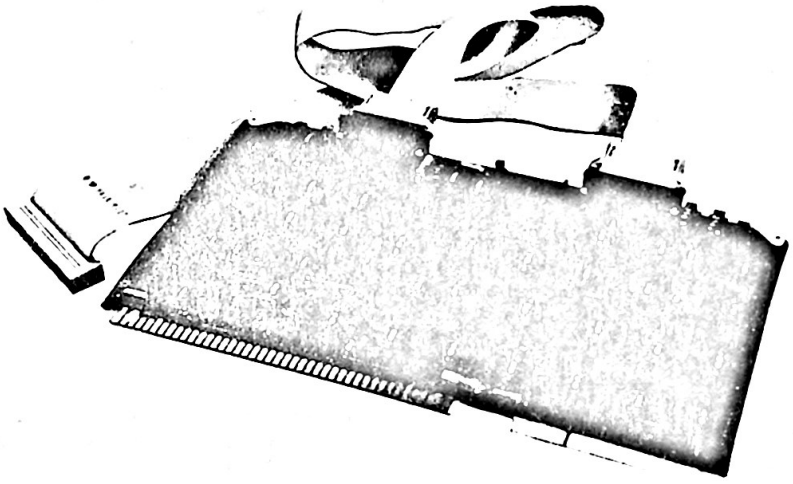
Figure 1. COP2440 Architecture

DA-B25M81/Printed in U.S.A.

National Semiconductor

November 1981

COPS™ In-System Emulator (ISE™) Package



- **True Real-Time Emulation of the COP400 Family of Microcontrollers**
- **Plugs Directly into Any STARPLEX™/STARPLEX II™ Development System**
- **Compatible with the Required Optional COP400 Family Emulator Boards**
- **Easy to Use**
  - Hardware
    - Real-time trace of 256 × 20-bit instruction cycles
    - 4K × 8-bit of Shared RAM Memory for rapid downloading of programs from STARPLEX/STARPLEX II peripherals
    - 1K × 12-bit dump memory used in place of control firmware
    - External hardware breakpoint
    - Breakpoint timer in milliseconds
    - Fully compatible with a STARPLEX/ STARPLEX II system bus
    - One target card handles entire series of microcontrollers and COP400 Emulator Boards
  - Software
    - Software breakpoints
    - Lists user-specified registers when selected breakpoint is detected
    - Mnemonic modification of object code
    - Step-list-restart command
    - Dump routines for various COPS microcontroller chips
- **Compatible Software Available to Control the COPS-T01 QUIKLOOK™ Incoming Component Tester**

Product Overview

The COP400 In-System Emulator (ISE) is designed for users with the STARPLEX/STARPLEX II Development System. Coupled with the power of STARPLEX/ STARPLEX II, COP400 ISE is a very powerful tool available for developing and debugging COP400 family based microcontroller products. The COP400 ISE target board plugs directly into any STARPLEX/STARPLEX II Development System and interfaces easily with any COP400 system. The designer has the capability of executing the target system program in real-time while collecting up to 256 instruction cycles of true real-time trace data. In addition, he can single step through his program and display the data from a 4K Shared Memory location.

Circle DATA UPDATE No. 950502

AG-B 30M 1111 /Printed in U S A

National Semiconductor

October 1980

COPS QUIKLOOK™ TESTER: COP400-TO1

Supports the Entire COP400 Microcontroller Family

- **Hardware:**

  Tester Chassis, Component Interface Cards (4), Diagnostic Card, Development System/Quik-look Cables (2)

- **Software:**

  Master diskette contains programs for use with COP400-PDS Development System

Easy to Use Features

- Tester Diagnostics
- Automatic Chip Handler Interface
- Test Generation Program

Product Overview

The COPS QUIKLOOK TESTER provides a simple but effective means to perform incoming inspection of the National Semiconductor Corporation COP400 family. The QUIKLOOK TESTER, under the control of the COP400-PDS Development System, provides GO, NO-GO functional tests for COP400 devices.

Comprehensive Test Capability

The following COP400 features are tested at 5 Volts

a) Maximum frequency operation
b) Chip I/O functionality
c) Register/memory reference instructions
d) Arithmetic instructions
e) Branch instructions
f) ROM
g) RAM
h) CKO xtal output (optional)
i) Interrupts (optional)
j) Multicop sync (optional)
k) Low power reset (optional 444L/445L only) (4.3 volts)
l) Dual clock (optional 420C/421C only)
m) CKO as a general purpose input (optional)
n) RAM keep alive (optional)
o) MICROBUS™ (optional)

Diagnostics

Tests QUIKLOOK system hardware for correct operation

Test Generation Program

The test generation program is used to generate test patterns for comparison with incoming masked parts. The resulting patterns are stored on the development system diskette for loading into the QUIKLOOK TESTER at run time.

Order Information

COP400-TO1 (60 Hz 120 V_{AC})
COP400-TO1E (50 Hz 220 V_{AC})

Documentation

420306199-001 Operators Manual

Software

440306199-200 Master Diskette

Note: To be used with COPS Development System

COP400-PDS (60 Hz 120 V_{AC})
COP400-PDSE (50 Hz 220 V_{AC})

Environmental Requirements

Operating and Storage Temperature 50° to 125°F
Relative Humidity 8% to 80%
Maximum Wet Bulb Temperature 85°F

Shipping
Temperature −40° to 125°F
Relative Humidity 8% to 80%
Maximum Wet Bulb Temperature 85°F

Power
115 Volts AC ±10%, 60 Hz, 24 watts
230 volts AC ±10%, 50 Hz, 27.69 watts

Physical Specifications
Height 5¾", Width 14", Depth 15½"

DA-FL15M110/Printed in U.S.A.

National Semiconductor

July 1981

DAC1020 10-Bit Binary Multiplying D/A Converter
DAC1220 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

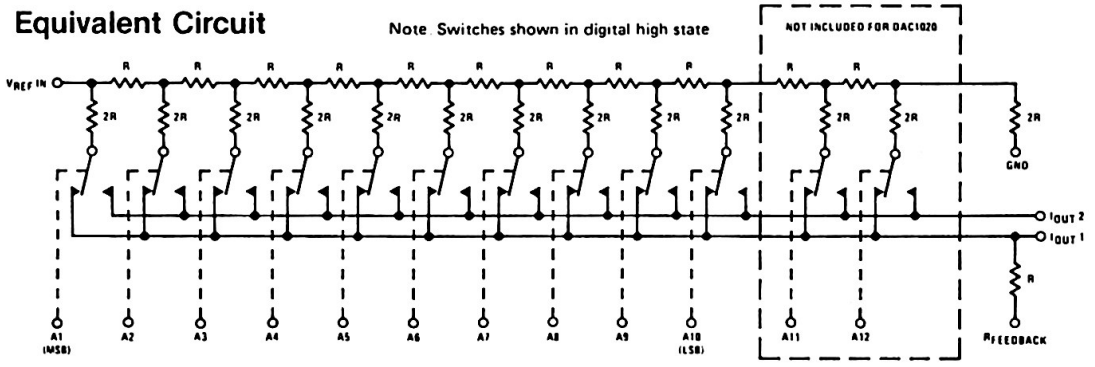
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guarenteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021 and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 and equivalent to the AD7533 family. The DAC1220, DAC1221 and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Linearity specified with zero and full-scale adjust only
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @ 15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq +25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



Ordering Information

10-BIT D/A CONVERTERS

TEMPERATURE RANGE		0 C to 70 C		40 C to +85 C		55 C to +125 C	
ACCURACY	0.05%	DAC1020LCN	AD7520LN AD7530LN	DAC1020LCD	AD7520LD AD7530LD	DAC1020LD	AD7520UD
	0.10%	DAC1021LCN	AD7520KN AD7530KN	DAC1021LCD	AD7520KD AD7530KD	DAC1021LD	AD7520TD
	0.20%	DAC1022LCN	AD7520JN AD7530JN	DAC1022LCD	AD7520JD AD7530JD	DAC1022LD	AD7520SD
PACKAGE OUTLINE		N16A		D16C		D16C	

12-BIT D/A CONVERTERS

TEMPERATURE RANGE		0 C to 70 C		40 C to +85 C		55 C to +125 C	
ACCURACY	0.05%	DAC1220LCN	AD7521LN AD7531LN	DAC1220LCD	AD7521LD AD7531LD	DAC1220LD	AD7521UD
	0.10%	DAC1221LCN	AD7521KN AD7531KN	DAC1221LCD	AD7521KD AD7531KD	DAC1221LD	AD7521TD
	0.20%	DAC1222LCN	AD7521JN AD7531JN	DAC1222LCD	AD7521JD AD7531JD	DAC1222LD	AD7521SD
PACKAGE OUTLINE		N18A		D18A		D18A	

Note. Devices may be ordered by either part number.

IM B25M71/Printed in U.S.A.

National Semiconductor

August 1981

DAC1285A, DAC1285 (DAC85, DAC87) 12-Bit Digital-to-Analog Converters

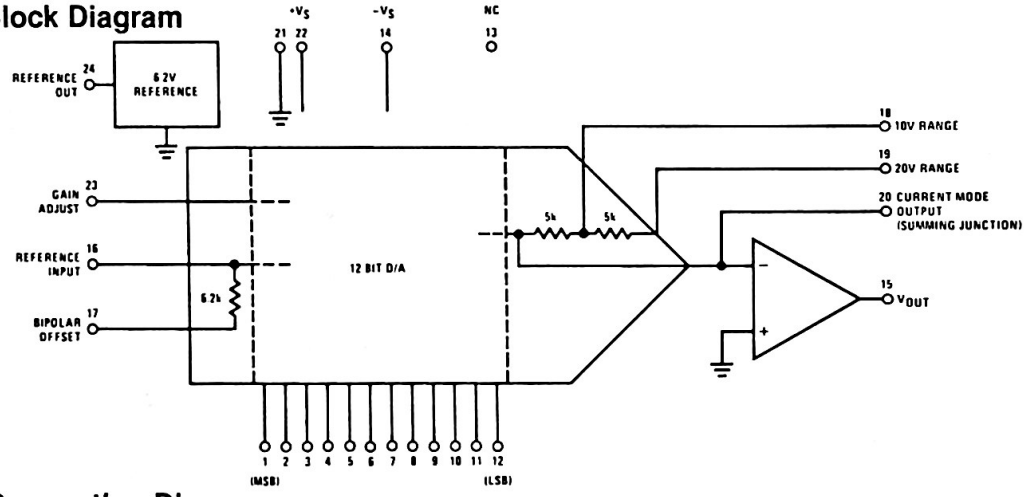
General Description

The DAC1285 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low (≤0.8V) turns a given bit ON, and a logic high (≥2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of ±2.5V, ±5V, ±10V, and unipolar ranges of 0V to 5V or 0V to 10V. Current mode output is 0 mA to 2 mA.

Features

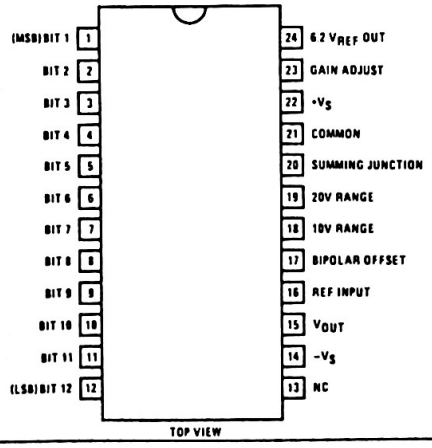
- Completely self-contained with internal reference and output amplifier
- High reliability exact replacement for DAC85-CBI-V, DAC85LD-CBI-V, and DAC87-CBI-V
- ± 1/2 LSB linearity max over temperature range
- ±2.5V, ±5V, ±10V, 0V to 5V, 0V to 10V voltage outputs
- 0 mA to 2 mA current output
- Fast settling time: 300 ns current mode; 2.5 μs voltage mode
- Hermetic 24-pin IC package
- Low cost
- TTL CMOS compatible binary input logic over temperature
- Parameters guaranteed over operating temperature range −25°C to +85°C or −55°C to +125°C

Block Diagram



Connection Diagram

Dual-In-Line Package



National Semiconductor

PRELIMINARY INFORMATION
JULY 1981

DP8340 Serial Bi-Phase Transmitter/Encoder

General Description

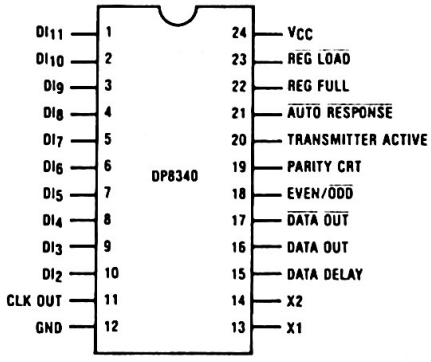
The DP8340 generates a complete encoding of parallel data for high speed serial transmission which conforms to the protocol as defined by the IBM 3270 information display system standard. The DP8340 converts parallel input data into a serial data stream. Although the IBM standard covers bi-phase serial data transmission over a coax line, the DP8340 also adapts to general high speed serial data transmission over other than coax lines, at frequencies either higher or lower than the IBM standard.

The DP8340 and its complementary chip, the DP8341 (receiver/decoder) have been designed to provide maximum flexibility in system designs. The separation of the transmitter/receiver functions provides convenient addition of more receivers at one end of a bi-phase line without the need of unused transmitters. This is specifically advantageous in control units where typical bi-phase data is multiplexed over many bi-phase lines and the number of receivers generally exceeds the number of transmitters.

Features

- Ten bits per data byte transmission
- Single-byte or multi-byte transmission
- Internal parity generation (even or odd)
- Internal crystal controlled oscillator used for the generation of all required chip timing frequencies
- Clock output directly drives receiver (DP8341) clock input
- Input data holding register
- Automatic clear status response feature
- Line drivers at data outputs provide easy interface to bi-phase coax line or general transmission lines
- Bipolar technology provides TTL input/output compatibility
- Internal power up clear and reset
- Single +5V power supply

Connection Diagram



Order Number:
DP8340N
DP8340J

Figure 1. Pin-Out Diagram

DA-B25K71/Printed in U.S.A.

National Semiconductor

PRELIMINARY INFORMATION
SEPTEMBER 1981

DP8342 High Speed Serial Transmitter/Encoder

General Description

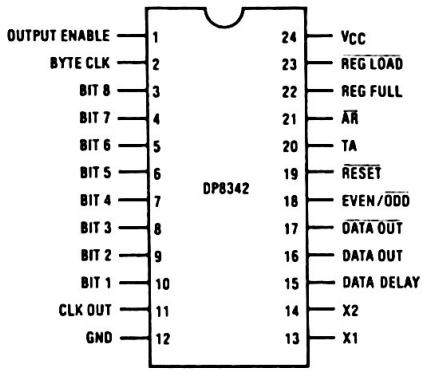
The DP8342 generates complete encoding of parallel data for high speed serial transmission. It generates a five bit starting sequence, three bit code violation, followed by a syn bit and eight bit per byte of data plus a parity bit. A three-bit ending code signals the termination of the transmission. The DP8342 adapts to generalized high speed serial data transmission as well as the coax lines at a maximum data rate of 3.5 MHz.

The DP8342 and its complementary chip, the DP8343 (receiver/decoder) have been designed to provide maximum flexibility in system designs. The separation of the transmitter/receiver functions provides convenient addition of more receivers at one end of a bi-phase line without the need of unused transmitters. This is specifically advantageous in control units where typical bi-phase data is multiplexed over many bi-phase lines and the number of receivers generally exceeds the number of transmitters.

Features

- Eight bits per data byte transmission
- Single-byte or multi-byte transmission
- Internal parity generation (even or odd)
- Internal crystal controlled oscillator used for the generation of all required chip timing frequencies
- Clock output directly drives receiver (DP8343) clock input
- Input data holding register
- Automatic clear status response feature
- Line drivers at data outputs provide easy interface to bi-phase coax line or general transmission media
- Bipolar technology provides TTL input/output compatibility
- Internal power up clear and reset
- Single +5V power supply

Connection Diagram



Order Number
DP8342N
DP8342J

Figure 1. Pin-Out Diagram

DA B10M91/Printed in U.S.A.

National Semiconductor

PRELIMINARY INFORMATION
JULY 1981

DP8343 High Speed Serial Receiver/Decoder

General Description

The DP8343 provides complete decoding of data for high speed serial data communications. In specific, the DP8343 receiver recognizes Bi-Phase serial data sent from its complementary chip, the DP8342 transmitter, and converts it into eight (8) bits of parallel data. These devices are easily adapted to generalized high speed serial data transmission systems that operate at bit rates up to 3.5 MHz.

The DP8343 receiver and the DP8342 transmitter are designed to provide maximum flexibility in system designs. The separation of transmitter and receiver functions allows addition of more receivers at one end of the Bi-Phase line without the necessity of adding unused transmitters. This is advantageous in control units where the data is typically multiplexed over many lines and the number of receivers generally exceeds the number of transmitters. The separation of transmitter and receiver function provides an additional advantage in flexibility of data bus organization. The data bus outputs of the receiver are TRI-STATE®, thus enabling the bus configuration to be organized as either a common transmit/receive (bi-directional) bus or as separate transmit and receive busses for higher speed.

Features

- DP8343 receives eight (8) bit data bytes
- Separate receiver and transmitter provide maximum system design flexibility
- Internal parity detection
- High sensitivity input on receiver easily interfaces to coax line
- Standard TTL data input on receiver provides generalized transmission line interface and also provides hysteresis
- Data holding register
- Multi-byte or single byte transfers
- TRI-STATE® receiver data outputs provide flexibility for common or separated transmit/receive data bus operation
- Data transmission error detection on receiver provides for both error detection and error type definition
- Bi-polar technology provides TTL input/output compatibility with excellent drive characteristics
- Single +5V power supply operation

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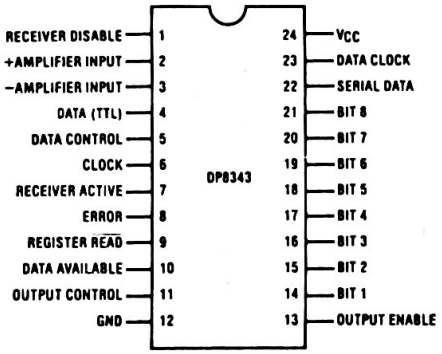
Connection Diagram



Order Number
DP8343N
DP8343J

Figure 1. Pin-Out Diagram

DA-B25K71/Printed in U.S.A.

National Semiconductor

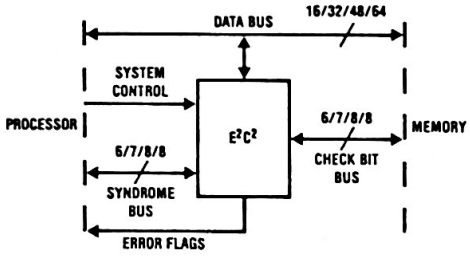
October 1981

ADVANCED INFORMATION

DP8400 — E^2C^2 Expandable Error Checker and Corrector

General Description

The DP8400 Expandable Error Checker and Corrector (E^2C^2) aids system reliability and integrity by detecting errors in memory data and correcting single or double-bit errors. The E^2C^2 data I/O port sits across the processor-memory data bus as shown, and the check bit I/O port connects to the memory check bits. Error flags are provided, and a syndrome I/O port is available. Fabricated using high speed Schottky technology in a 48-pin dual-in-line package, the DP8400 has been designed such that its internal delay times are minimal, maintaining maximum memory performance.



For a 16-bit word, the DP8400 monitors data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400 uses an encoding matrix to generate 6 check bits from the 16 bits of data. In a WRITE cycle, the data word and the corresponding check bits are written into memory. When the same location of memory is subsequently read, the E^2C^2 generates 6 new check bits from the memory data and compares them with the 6 check bits read from memory to create 6 syndrome bits. If there is a difference (causing some syndrome bits to go high), then that memory location contains an error and the DP8400 indicates the type of error with 3 error flags. If the error is a single-bit error, the DP8400 will automatically correct it.

The DP8400 is easily expandable to other data configurations. For a 32-bit data bus with 7 check bits, two DP8400s can be used in cascade with no other ICs. Three DP8400s can be used for 48 bits, and four DP8400s for 64 data bits, both with 8 check bits. In all these configurations, single and double-error detection and single-error correction are easy to implement.

When the memory is more unreliable, or better system integrity is preferred, then in any of these configurations, double-error correction can be performed. One approach requires a further memory WRITE-READ cycle using complemented data and check bits from the DP8400. If at least one of the two errors is a hard error, the DP8400 will correct both errors. This implementation requires no more memory check bits or DP8400s than the single-error correct configurations.

The DP8400 has a separate syndrome I/O bus which can be used for error logging or error management. In addition, the DP8400 can be used in BYTE-WRITE applications (for up to 72 data bits) because it has separate byte controls for the data buffers. In 16 or 32-bit systems, the DP8400 will generate and check system byte parity, if required, for integrity of the data supplied from or to the processor. There are three latch controls to enable latching of data in various modes and configurations.

Operational Features

- Fast single and double-error detection
- Fast single-error correction
- Double-error correction after catastrophic failure with no additional ICs or check bits
- Functionally expandable to 100% double-error correct capability
- Functionally expandable to triple-error detect
- Directly expandable to 32 bits using 2 DP8400s only
- Directly expandable to 48 bits using 3 DP8400s only
- Directly expandable to 64 bits using 4 DP8400s only
- Expandable to and beyond 64 bits in fast configuration with extra ICs
- 3 error flags for complete error recording
- 3 latch enable inputs for versatile control
- Byte parity generating and checking
- Separate byte controls for outputting data in BYTE-WRITE operation
- Separate syndrome I/O port accessible for error logging and management
- On-chip input and output latches for data bus, check bit bus and syndrome bus
- Diagnostic capability for simulating check bits
- Memory check bit bus, syndrome bus, error flags and internally generated syndromes available on the data bus
- Self-test of E^2C^2 on the memory card under processor control
- Full diagnostic check of memory with the E^2C^2
- Complete memory failure detectable
- Power-on clears data and syndrome input latches

Timing Features

16-BIT CONFIGURATION

WRITE Time: 23 ns from data-in to check bits valid
DETECT Time: 21 ns from data-in to Any Error (AE) flag set
CORRECT Time: 35 ns from data-in to correct data out

IM-B25M101/Printed in U.S.A

National Semiconductor

ADVANCED INFORMATION
DECEMBER 1981

DP8408 Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC. . . the DP8408 Dynamic RAM Controller/Driver. The DP8408 is capable of driving all 16k and 64k Dynamic RAMs (DRAMs). Since the DP8408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8408's 6 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing less complicated; and automatic memory initialization is both simple and fast.

The DP8408 is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and control signals. It consists of two 8-bit address latches, an 8-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 20 ns. The DP8408 timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8408 has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{\text{REFRESH}}$. These 3 pins select 6 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{\text{RAS}}$ outputs. During normal access, the 8 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 8-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected, while $\overline{\text{CAS}}$ is inhibited.

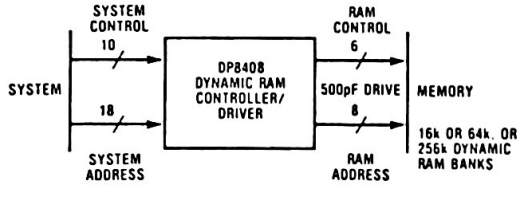
The DP8408 can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, or 64k's. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.

Operational Features

- All DRAM drive functions on one chip — minimizes skew on outputs, maximizes AC performance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drives directly all 16k and 64k DRAMs
- Capable of addressing 64k and 256k words
- Propagation delays of 20 ns typical at 500 pF load
- $\overline{\text{CAS}}$ goes low automatically after column addresses are valid if desired
- Auto access mode provides $\overline{\text{RAS}}$, Row to Column select then $\overline{\text{CAS}}$ automatically and fast
- $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally—offering READ, WRITE, and READ-MODIFY-WRITE cycles
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- End-of-Count indicated by RF I/O pin going low at 127 or 255
- Low input on RF I/O resets 8-bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

- 6 modes of operation: 3 access, 1 refresh, and 2 set-up
- 2 externally controlled modes: 1 access (Mode 4) and 1 refresh (Modes 0, 1, 2)
- 2 auto-access modes $\overline{\text{RAS}} \rightarrow \text{R}/\overline{\text{C}} \rightarrow \overline{\text{CAS}}$ automatic, with $t_{\overline{\text{RAH}}}$ = 20 or 30 ns minimum (Modes 5, 6)
- Externally controlled All-$\overline{\text{RAS}}$ Access modes for memory initialization (Mode 3)
- End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)



DP8408 Interface Between System & DRAM Banks

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DA-SVP20081/Printed in U.S.A.

National Semiconductor

ADVANCED INFORMATION
DECEMBER 1981

DP8409 Multi-Mode Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC. . . the DP8409 Multi-Mode Dynamic RAM Controller/Driver. The DP8409 is capable of driving all 16k and 64k Dynamic RAMs (DRAMs) as well as 256k DRAMs. Since the DP8409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8409's 8 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The DP8409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 20 ns. The DP8409 timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8409 has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{\text{REFRESH}}$. These 3 pins select 8 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{\text{RAS}}$ outputs. During normal access, the 9 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 9-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected, while $\overline{\text{CAS}}$ is inhibited.

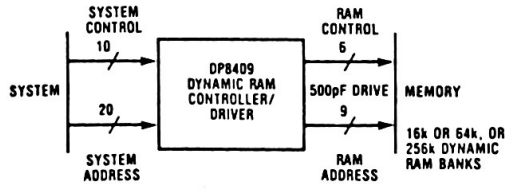
The DP8409 can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, 64k's, or 256k's. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.

Operational Features

- All DRAM drive functions on one chip — minimizes skew on outputs, maximizes AC performance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drives directly all 16k, 64k, and 256k DRAMs
- Capable of addressing 64k, 256k, or 1M words
- Propagation delays of 20 ns typical at 500 pF load
- $\overline{\text{CAS}}$ goes low automatically after column addresses are valid if desired
- Auto Access mode provides $\overline{\text{RAS}}$, Row to Column select, then $\overline{\text{CAS}}$ automatically and fast
- $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally—offering READ, WRITE or READ-MODIFY-WRITE cycles
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255, or 511)
- End-of-Count indicated by RF I/O pin going low at 127, 255, or 511
- Low input on RF I/O resets 9-bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

- 8 modes of operation: 3 access, 3 refresh, and 2 set-up
- 2 externally controlled modes: 1 access and 1 refresh (Modes 0, 4)
- 2 auto-access modes $\overline{\text{RAS}}$ → R/$\overline{\text{C}}$ → $\overline{\text{CAS}}$ automatic, with t_{RAH} = 20 or 30 ns minimum (Modes 5, 6)
- Auto-access mode allows Hidden Refreshing (Mode 5)
- Forced Refresh requested on RF I/O if no Hidden Refresh (Mode 5)
- Forced Refresh performed after system acknowledge of request (Mode 1)
- Automatic Burst Refresh mode stops at End-of-Count of 127, 255, or 511 (Mode 2)
- 2 All-$\overline{\text{RAS}}$ Access modes externally or automatically controlled for memory initialization (Modes 3a, 3b)
- Automatic All-$\overline{\text{RAS}}$ mode with external 8-bit counter frees system for other set-up routines (Mode 3a)
- End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)



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Circle DATA UPDATE No. 950504

DA SVP20081/Printed in U S A

National Semiconductor

PRELIMINARY
SEPTEMBER 1981

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

General Description

The DP84240 and DP84244 are octal TRI-STATE® drivers which are ideally suited as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 50 pF and 500 pF load capacitances.

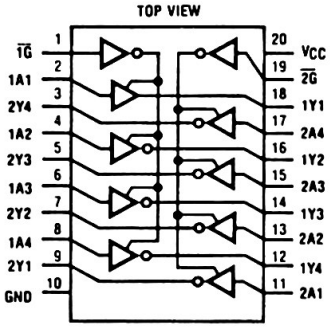
Features

- t_{pd} specified with 50 pF and 500 pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500 pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters fully tested

TRI-STATE is a registered trademark of National Semiconductor Corporation

Connection Diagrams

TOP VIEW



Truth Tables

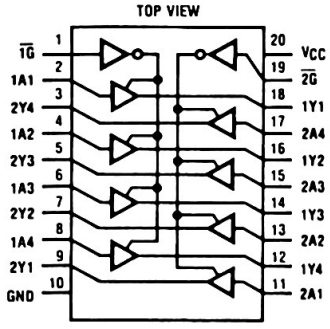
DP84240

Inputs $\overline{G}$	A	Outputs Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244

TOP VIEW



Inputs $\overline{G}$	A	Outputs Y
H	X	Z
L	L	L
L	H	H

DA-B25M91/Printed in U.S.A.

National Semiconductor

August 1981

DT1056/DT1057 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1056/DT1057 is a standard DIGITALKER kit encoded with 131 separate and useful words (see the Master Word List Table I) and when used with the DT1050 Standard Vocabulary Kit, provides a library of 274 useful words. The words have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1056/DT1057 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

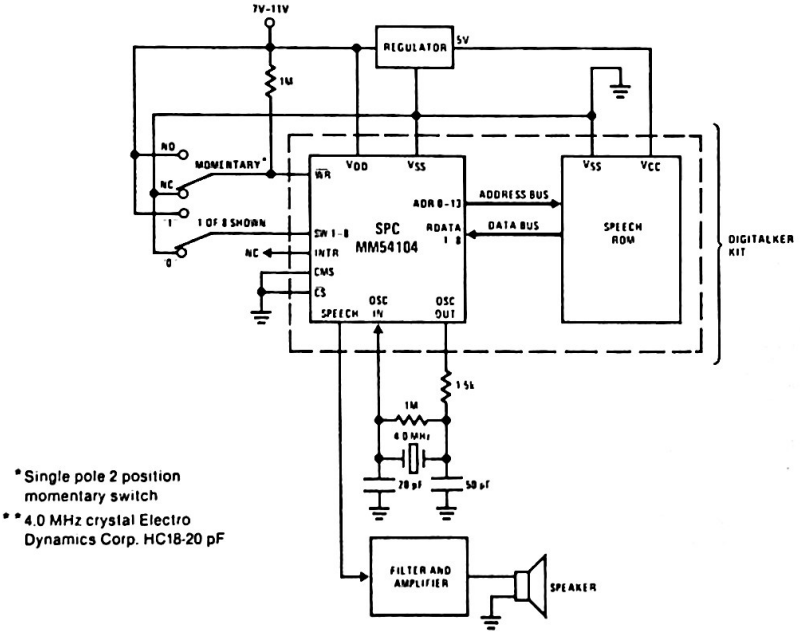
- Easily adaptable to DT1050 Standard Vocabulary Kit
- 131 useful words
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- Natural inflection and emphasis of original speech
- Addresses 128k bits of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Available in complete kit (DT1056) or speech ROMs only (DT1057)

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp. HC18-20 pF

IM-B25M81/Printed in U.S.A.

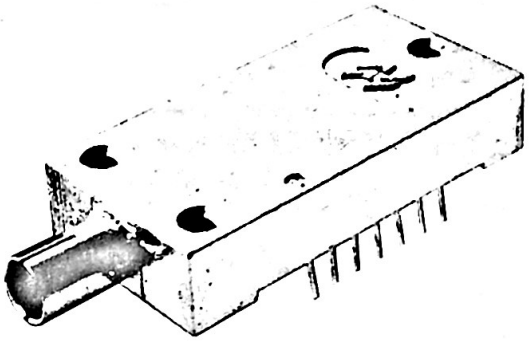
National Semiconductor

ADVANCE INFORMATION
SEPTEMBER 1981

FOR100B Fiber-Optic Receiver

General Description

The FOR100B is a general-purpose fiber-optic receiver. It contains a low-capacitance pin photodiode, FET-input transimpedance preamplifier and a comparator with hysteresis. An integral self-aligning bayonet-style connector simplifies and ensures reliable optical coupling. The low profile metal package is ideal for direct PC board mounting with 0.5" board-to-board spacing. When used with the FOT180B fiber-optic transmitter, the pair will provide a complete fiber-optic data link capable of 5 Mbits/s NRZ data rate with only 2 μW peak optical power input at the receiver. Connectors are available from Amphenol™.



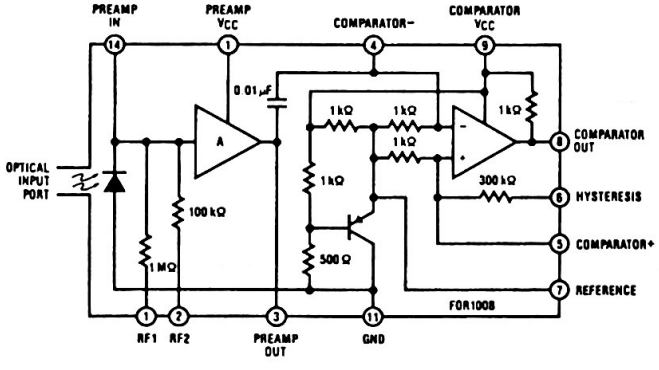
Features

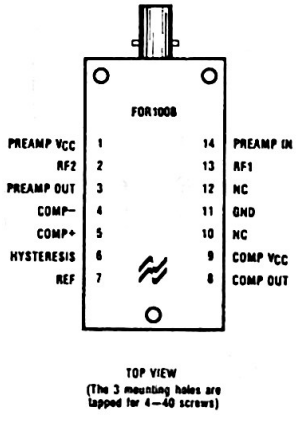
- Single 4.5V to 12V supply
- DC to 5 Mbits/s NRZ data bandwidth
- $<10^{-9}$ bit error rate
- Low capacitance silicon pin photodiode
- Pin selectable sensitivity
- CMOS/TTL compatible logic output
- >21 dB dynamic range (see Note 1, page 2)
- Quickly demountable bayonet-type Amphenol connector
- Separate analog and digital outputs
- 14-pin low-profile (0.3") package for direct PC board mounting

Applications

- Data communication networks
- Secure communications
- Peripheral control/communications
- Video transmission
- Optical modems
- Fiber-optic repeater
- Industrial machine control

Schematic and Connection Diagrams





TOP VIEW
(The 3 mounting holes are tapped for 4—40 screws)

Amphenol is a trademark of Amphenol Division, Bunker Ramo Corp.

DA-B25M111/Printed in U.S.A.

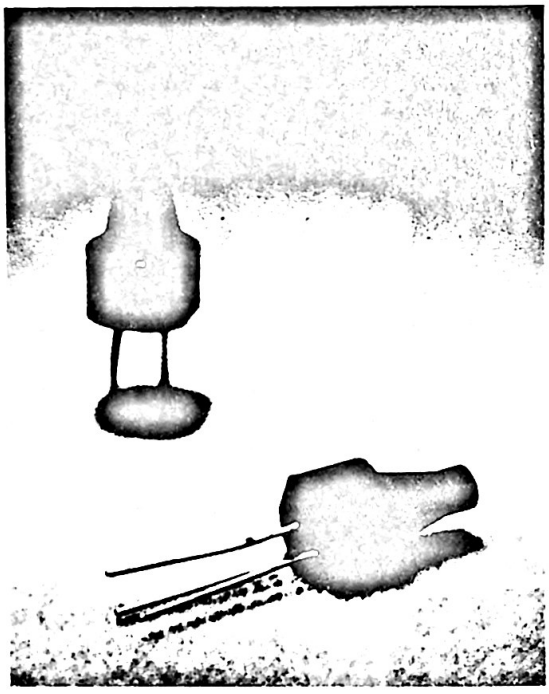
National Semiconductor

ADVANCE INFORMATION
SEPTEMBER 1981

FOR261F Monolithic TTL Fiber-Optic Receiver

General Description

The FOR261F is a high speed monolithic fiber -optic receiver accepting optical input and providing TTL outputs at NRZ data rates to 10 Mbits/s with only 7 μW of optical power. It is available in a short ferrule package which is compatible with Amphenol™ and AMP™ standard receptacles.



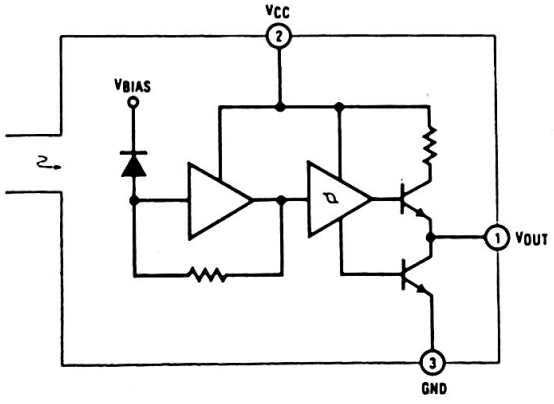
Features

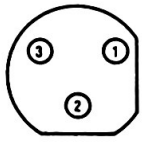
- Single +5V supply
- Optical input, TTL output
- 10 Mbits/s NRZ data rate with only 7 μW of peak optical power
- $<10^{-9}$ bit error rate
- Short ferrule package with 250 μm diameter optical port
- Compatible with AMP #227240-1 and Amphenol #905-135-5000 connectors
- Temperature compensated input

Applications

- Data communications
- Optical modem
- Industrial machine control
- Peripheral control/communications

Equivalent Circuit and Connection Diagram





Bottom View

AMP is a trademark of AMP Corp.
Amphenol is a trademark of Bunker Ramo Corp.

DA-B25M111/Printed in U.S.A.

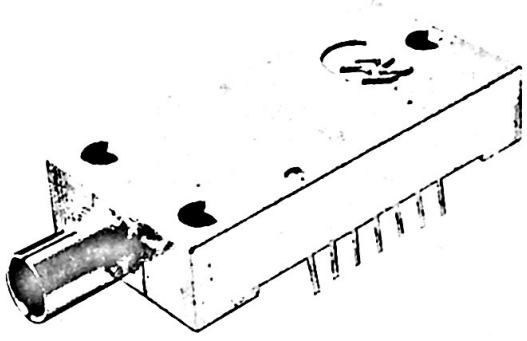
National Semiconductor

ADVANCE INFORMATION
SEPTEMBER 1981

FOT180B Fiber-Optic Transmitter

General Description

The FOT180B is a high-speed general-purpose electro-optical transmitter. It is designed for digital data transmission via optical fibers with data rates up to 20 MBits/s NRZ. The package includes the driver circuitry, optical light source, and connector. The bayonet-type connector on the package simplifies and ensures reliable optical coupling with minimal source to fiber alignment losses. The low-profile metal package is ideal for direct PC board mounting with 0.5" board-to-board spacing. When used with the FOR100B fiber-optic receiver, the pair provides a complete optical data link with TTL compatible interfacing. Connectors are available from Amphenol™.



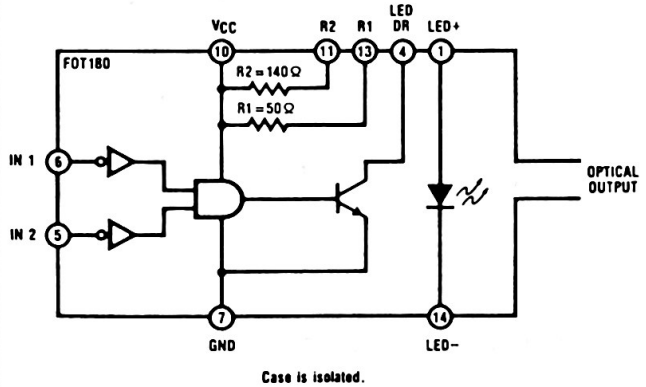
Features

- Single +5 V supply
- DC to 20 Mbits/s NRZ data rate
- Pin selectable optical output power
- LED built-in
- CMOS/TTL compatibility
- Data and enable inputs
- Quickly demountable bayonet-type Amphenol optical connector
- 14-pin low profile package (0.3") for direct PC board mounting
- Open collector output driver

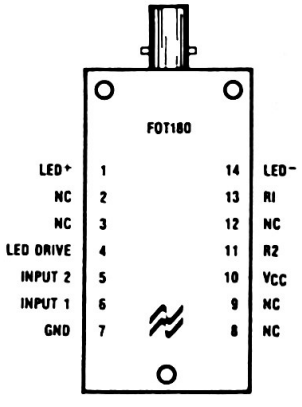
Applications

- Data communication networks
- Secure communications
- Peripheral control/communication
- Industrial machine control
- T1 and T2 telecom digital links
- Optical modems
- Video transmission

Schematic and Connection Diagram



Case is isolated.



TOP VIEW
(The 3 mounting holes are tapped for 4–40 screws)

Amphenol is a trademark of Amphenol Division, Bunker Ramo Corp See Page 13 25 for part number

DA-B25M111/Printed in U.S.A

National Semiconductor

PRELIMINARY INFORMATION
AUGUST 1981

High Performance Programmable Array Logic (PAL®) Family

General Description

The high performance PAL® family utilitzes National Semiconductor's Advanced Schottky TTL process and Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PALs is 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array.) In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, one additional fuse may be blown to make verification difficult. This feature gives the user a proprietary circuit which is very difficult to copy.

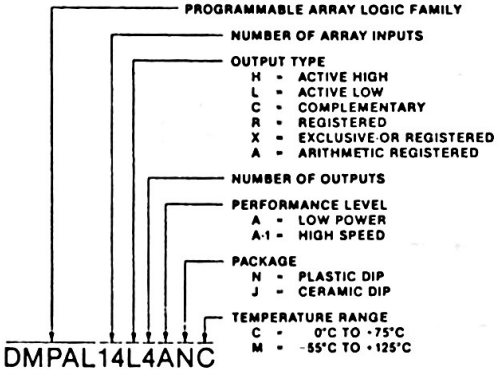
Features

- Programmable replacement for conventional TTL logic.
- Simplifies prototyping and board layout.
- 20-pin DIP packages.
- Programmed on standard PROM programmers.
- Special feature reduces possibility of copying by competitors.
- Reliable titanium-tungsten fuses.
- Low Power/High Speed Versions

"PAL" is a trademark of and used under license with Monolithic Memories, Inc

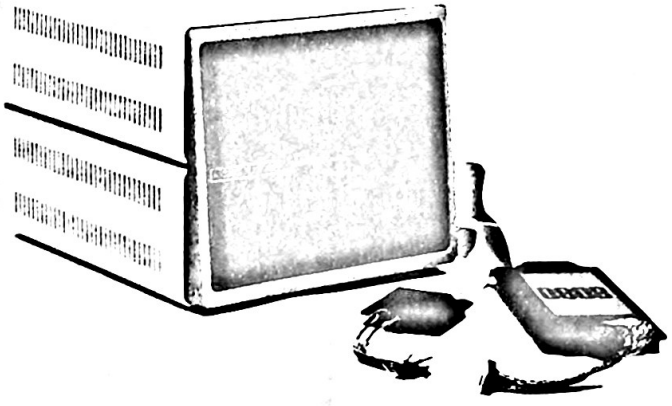
Ordering Information

BASIC PART NUMBER	DESCRIPTION
PAL10H8	OCTAL 10 INPUT AND-OR GATE ARRAY
PAL12H6	HEX 12 INPUT AND-OR GATE ARRAY
PAL14H4	QUAD 14 INPUT AND-OR GATE ARRAY
PAL16H2	DUAL 16 INPUT AND-OR GATE ARRAY
PAL16C1	16 INPUT AND-OR-AND-OR-INVERT GATE ARRAY
PAL10L8	OCTAL 10 INPUT AND-OR-INVERT GATE ARRAY
PAL12L6	HEX 12 INPUT AND-OR-INVERT GATE ARRAY
PAL14L4	QUAD 14 INPUT AND-OR-INVERT GATE ARRAY
PAL16L2	DUAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16L8	OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16R8	OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R6	HEX 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R4	QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY



DA-B15M81/Printed in U.S.A.

In-System Emulator™



- **A Total Emulation System**
  - Hardware
    - — CPU
    - — Breakpoint, trace, interface, memory mapping and control logic
    - — 32K byte memory
    - — Emulation processor
    - — RS232C serial port
  - Software
    - — Host resident symbolic debugger and driver software
    - — Control firmware
  - Options
    - — Target cards for 8080, 8048 family and 8070 family
    - — Cross Assemblers for 8048 family and 8070 family
- **Easy to Use**
  - Hardware
    - — 128 x 40-bit trace memory
    - — Memory mapping for 64 K byte address space
    - — 35 breakpoint conditions
    - — Coast after breakpoint
    - — Breakpoint and trace load sync pulses
    - — 8-bit user status cable
    - — Microsecond timer
  - Software
    - — Symbolic debugger
    - — In-line assembler
    - — Disassembler
    - — Automatic test
    - — Full access to STARPLEX™ Development System facilities
- **Versatile**
  - Single or double microprocessor emulation
  - Variety of microprocessors supported
  - Operates with STARPLEX™ Development System

Product Overview

National Semiconductor's In-System Emulator goes beyond the single-card approach to emulation and qualifies as a genuine innovation in the development of microprocessor-based systems.

ISE is a complete stand-alone unit housing 32K bytes of user programmable memory and all the necessary logic for breakpoints, tracing and memory mapping. Microprocessor emulation is isolated on a single target card containing all the logic needed to emulate the particular microprocessor. ISE is capable of supporting two of these target cards concurrently to achieve emulation in a multiprocessor environment. ISE can support either two target cards for the same microprocessor or two different microprocessors.

DA B10M71/Printed in U.S.A.

National Semiconductor

AUGUST 1981

LH0086/LH0086C Digitally-Programmable-Gain Amplifier

General Description

The LH0086 is a self-contained, high-accuracy, digitally-programmable-gain amplifier. It consists of a FET-input operational amplifier, a precision resistor ladder, and a digitally-programmable switch network. A three-bit TTL-compatible digital input selects accurate gain settings of 1, 2, 5, 10, 20, 50, 100, or 200.

The LH0086 exhibits low offset voltage, high input impedance, fast settling, high power supply rejection ratio, and excellent gain accuracy and gain non-linearity.

The LH0086 is specified for operation from −55°C to +125°C. The LH0086C is specified from −25°C to +85°C. Both devices are hermetically sealed in a 14-lead dual-in-line metal package.

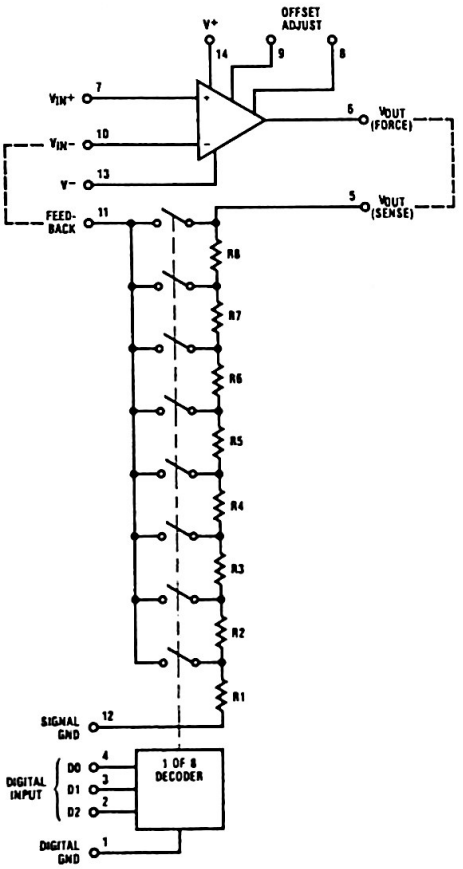
Features

- 0.01% gain accuracy at gain = 1
- 0.005% gain non-linearity
- 1ppm/°C typical gain drift
- $10^{10}\Omega$ input impedance
- 80dB minimum PSRR.
- TTL-compatible digital inputs
- 2μs settling to 0.01%

Applications

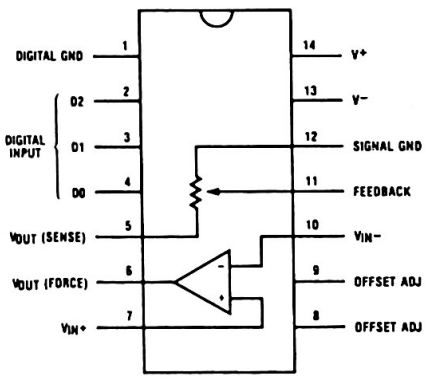
- Data acquisition systems
- Auto range DVMs
- Adaptive servo loops

Simplified Schematic



Connection Diagram

Dual-In-Line Package



CASE IS ELECTRICALLY ISOLATED

Top View

DA-B25M81/Printed in U.S.A.

National Semiconductor

NOVEMBER 1981

LH1605 5 Amp, High Efficiency Switching Regulator

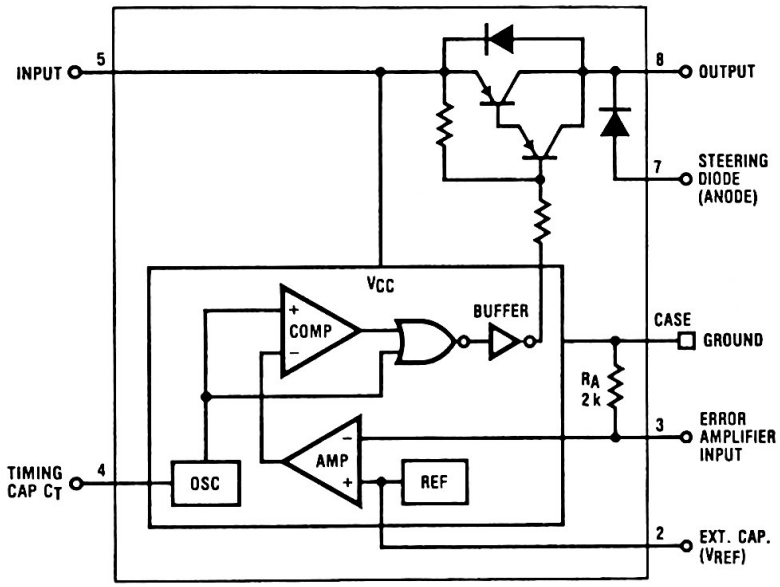
General Description

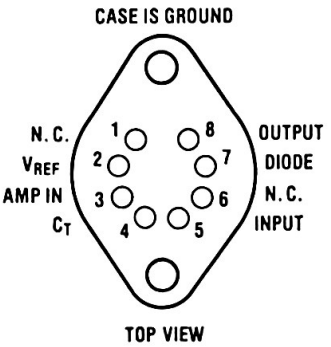
The LH1605 is a hybrid switching regulator with high output current capability. It incorporates a temperature-compensated voltage reference, a duty cycle modulator with the oscillator frequency programmable, error amplifier, high current-high voltage output switch, and a power diode. The LH1605 can supply up to 5A of output current over a wide range of regulated output voltages.

Features

- Step down switching regulator
- Output adjustable from 3.0 to 30V
- 5A output current
- High efficiency
- Frequency adjustable to 100kHz
- Standard 8-pin TO-3 package

Block Diagram and Connection Diagram





Order Numbers
LH1605K
LH1605CK

Circle DATA UPDATE No. 950501

DAB25M111/Printed in U.S.A.

National Semiconductor

LM137/LM237/LM337 3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM237/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM237/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM237/LM337 are ideal complements to the LM117/LM217/LM317 adjustable positive regulators.

Features

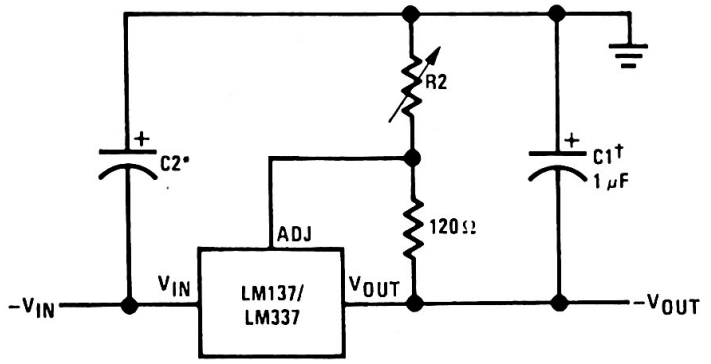
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

LM137 Series Packages and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM137 LM237 LM337	TO-3	20W	1.5A
	TO-39	2W	0.5A
LM337T	TO-220	15W	1.5A
LM337M	TO-202	7.5W	0.5A
LM337LZ	TO-92	6.2W	0.1A

Typical Applications

Adjustable Negative Voltage Regulator



$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability
*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

DA-B25M91/Printed in U.S.A.

National Semiconductor

August 1981
PRELIMINARY

LM163/LM363 Precision Instrumentation Amplifier

General Description

The LM163 is a monolithic true instrumentation amplifier. It requires no external parts for fixed gains of 10, 100 and 1,000. High precision is attained by on-chip trimming of offset voltage and gain. A super beta bipolar input stage gives very low input voltage noise, extremely low offset voltage drift, and high common-mode rejection ratio. A new two-stage amplifier design yields an open loop gain of 10,000,000 and a gain bandwidth product of 30 MHz, yet remains stable for all closed loop gains, even with large capacitive loads. Supply voltage range is ±5V to ±18V.

The LM163 has separate force, sense, and reference pins to allow gain to be increased using external resistors. Twin differential shield drivers eliminate bandwidth loss due to shield capacitance. Compensation pins are available to allow simple low-pass filtering. The LM163 with all options is in a 16-pin dual-in-line package.

For less stringent applications requiring a single fixed gain, it is also available in an 8-pin TO-5 package. Shield drivers, pin-strapped gain options, and offset adjustment pins are eliminated on the 8-pin versions. Gain is internally set at 10, 100, or 500, but may be increased with the addition of external resistors.

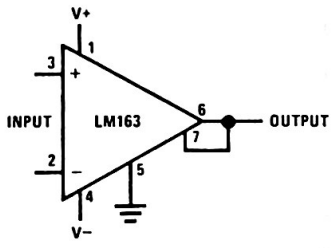
The LM163 is rated for −55°C to +125°C operation. The LM363 is rated for 0°C to 70°C operation.

Features

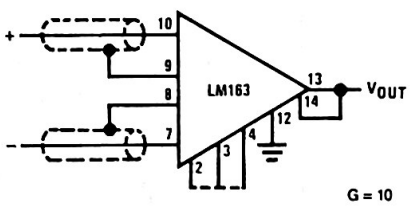
- Offset and gain pretrimmed
- 7 nV/√Hz input noise
- 130 dB CMRR typical
- 2 nA bias current typical
- No external parts required
- Differential shield drivers
- Available at 0.5 μV/°C maximum drift
- Can be used as a high performance op-amp

Typical Connections

8-Pin Package



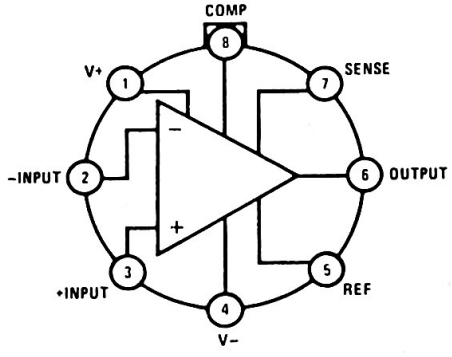
16-Pin Package



G = 10 2, 3, 4, open
G = 100 3-4 shorted
G = 1000 2-4 shorted

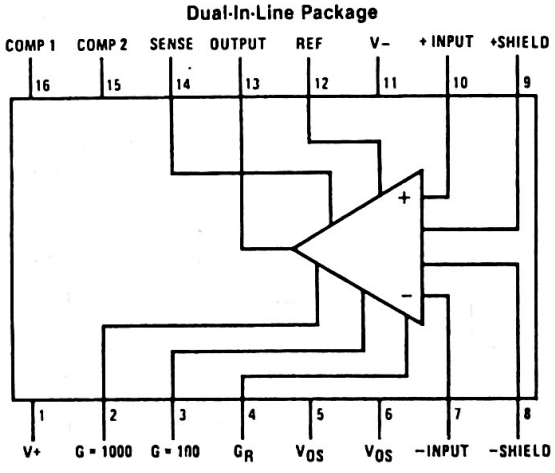
Connection Diagrams

Metal Can Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

IM-B25M81/Printed in U.S.A.

National Semiconductor

LM185-1.2/LM285-1.2/LM385-1.2 Micropower Voltage Reference Diode

General Description

The LM185-1.2/LM285-1.2/LM385-1.2 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

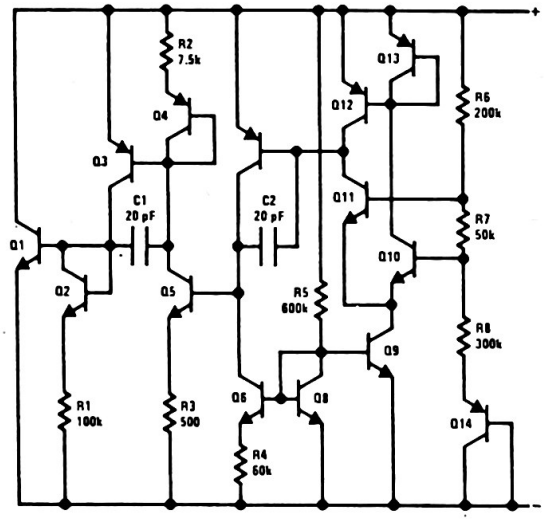
Careful design of the LM185-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation. Some outstanding features are:

- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—1.235V
- 2.5V device also available — LM385-2.5

The extremely low power drain of the LM185-1.2 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

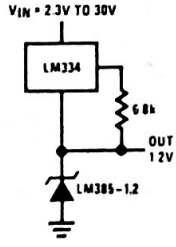
The LM185-1.2 is rated for operation over a −55°C to 125°C temperature range while the LM285-1.2 is rated −25°C to 85°C and the LM385-1.2 0°C to 70°C. The LM185-1.2/LM285-1.2/LM385-1.2 are available in a hermetic TO-46 package and the LM385-1.2 is also available in a low-cost TO-92 molded package.

Schematic Diagram

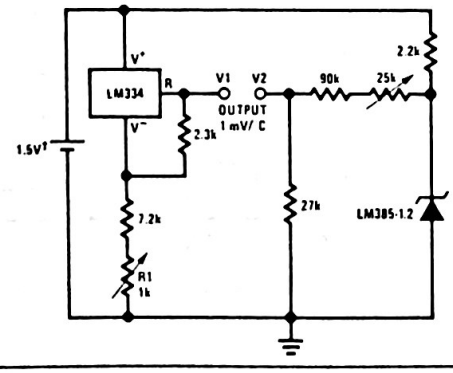


Applications

Wide Input Range Reference



Centigrade Thermometer



Calibration

1. Adjust R1 so that V1 = temp at 1 mV/°K
2. Adjust V2 to 273.2 mV

I_Q for 1.3V to 1.6V battery voltage = 50 μA to 150 μA

IM-B25M81/Printed in U.S.A.

LM185-1.2/LM285-1.2/LM385-1.2 Micropower Voltage Reference Diode

PAL® DATABOOK

DESCRIPTION

This book is intended to be a complete reference for the design of digital systems using Programmable Array Logic (PAL) devices. In addition to data sheets for all currently available devices, this book also contains extensive application notes intended to give design examples for a number of PAL devices. It also contains a step-by-step procedure for PAL design and programming, including the listing for PALASM™ which is a FORTRAN IV program that converts logic equations to PAL programming information.

Portions of this book have been reprinted with the permission of Monolithic Memories Inc., the originator of the PAL concept.

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National Semiconductor

July 1981

LM317L 3-Terminal Adjustable Regulator

General Description

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM317L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM317L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

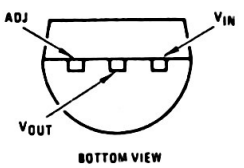
Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM317L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

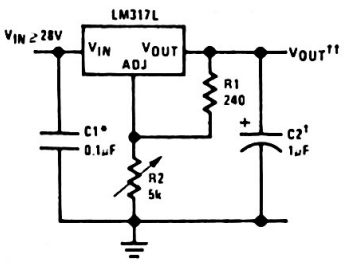
The LM317L is packaged in a standard TO-92 transistor package. The LM317L is rated for operation over a −25°C to 125°C range.

Connection Diagram



Typical Applications

1.2V-25V Adjustable Regulator

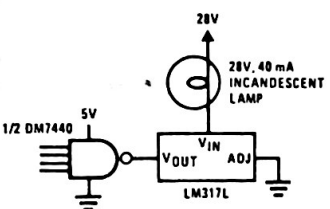


† Optional—improves transient response

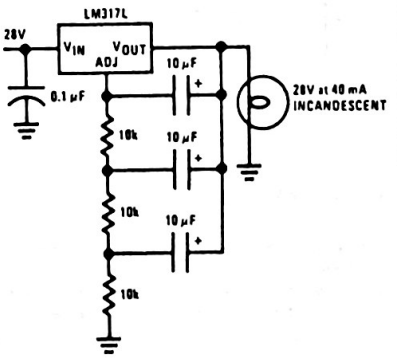
* Needed if device is far from filter capacitors

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

Fully Protected (Bulletproof) Lamp Driver



Lamp Flasher



Output rate — 4 flashes per second at 10% duty cycle

IM-B25M71/Printed in U.S.A.

National Semiconductor

August 1981
PRELIMINARY

LM337L 3-Terminal Adjustable Regulator

General Description

The LM337L is an adjustable 3-terminal negative voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators. Also, the LM337L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM337L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, only a single 1 μF solid tantalum output capacitor is needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. A larger output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

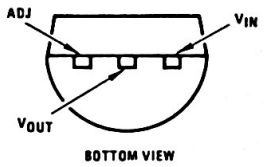
Besides replacing fixed regulators, the LM337L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM337L is packaged in a standard TO-92 transistor package. The LM337L is rated for operation over a −25°C to +125°C range.

For applications requiring greater output current in excess of 0.5A and 1.5A, see LM137 series data sheets. For the positive complement, see series LM117 and LM317L data sheets.

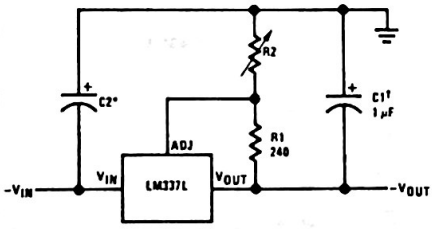
Connection Diagram



BOTTOM VIEW

Typical Applications

1.2V-25V Adjustable Regulator

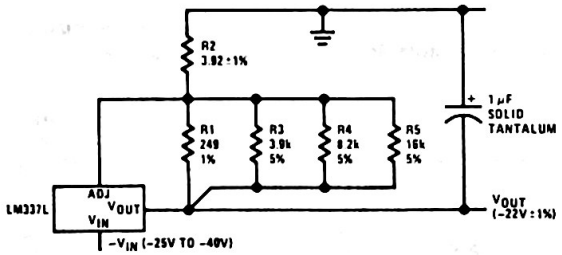


$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{240\Omega}\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power supply filter capacitor

Regulator with Trimmable Output Voltage



Trim Procedure:

—If V_{OUT} is −23.08V or bigger, cut out R3 (if smaller, don't cut it out).

—Then if V_{OUT} is −22.47V or bigger, cut out R4 (if smaller, don't).

—Then if V_{OUT} is −22.16V or bigger, cut out R5 (if smaller, don't).

This will trim the output to well within 1% of −22.00 V_{DC}, without any of the expense or trouble of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

IM-B25M81/Printed in U.S.A.

National Semiconductor

September 1981

LM2111 FM Detector and Limiter

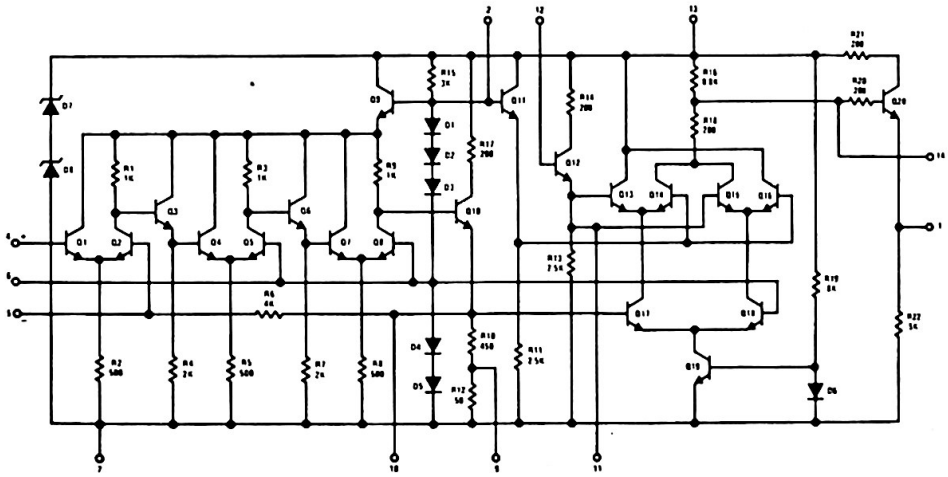
General Description

The LM2111 is a monolithic integrated circuit FM detector and limiter that requires a minimum of external components for operation. It includes three stages of IF limiting and a balanced product detector.

Features

- A direct replacement for ULN2111A and MC1357
- Simple detector alignment: one coil or ceramic filter
- Sensitivity: 3 dB limiting voltage 300 μV typ.
- Low harmonic distortion
- High IF voltage gain

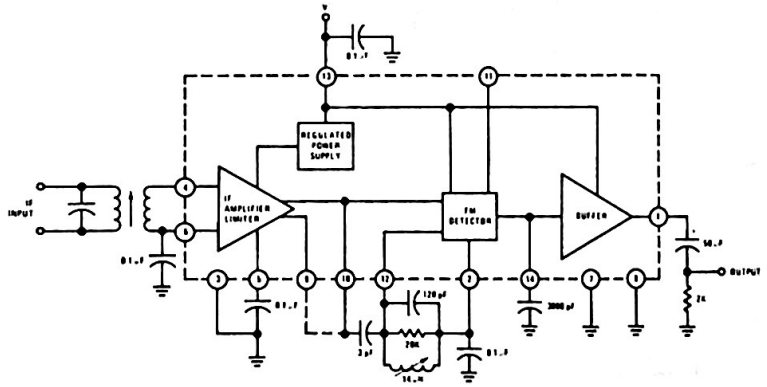
Schematic Diagram



Order Number LM2111N
See NS Package N14A

Block Diagram

Order Number LM2111N-01
See NS Package N14C



IM-B20M91/Printed in U.S.A.

September 1981

National Semiconductor

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to 1/2%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

Features

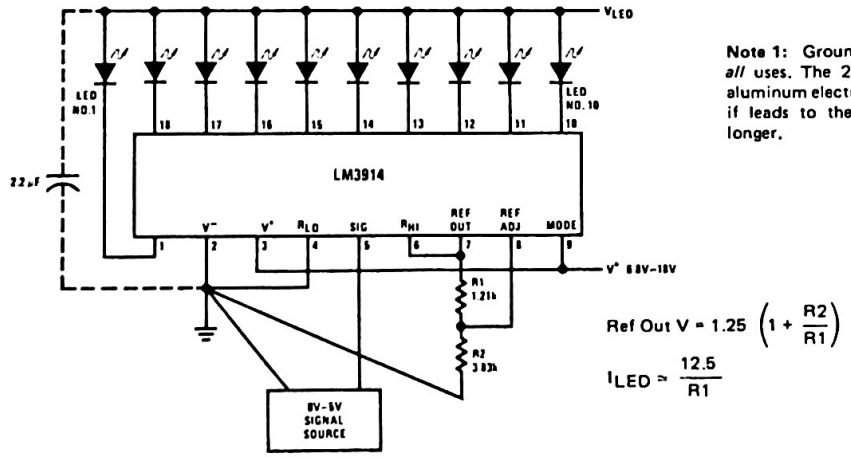
- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package and the LM3914J comes in the 18-lead ceramic DIP.

The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Typical Applications

0V to 5V Bar Graph Meter



Note 1: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \simeq \frac{12.5}{R1}$$

IM-B25M91/Printed in U.S.A.

National Semiconductor

October 1981

LT10 Linear Bipolar Power Transistor

general description

The LT10 is an entirely new power transistor design that combines exceptional ruggedness with an $f_T > 40$ MHz. Forward biased secondary breakdown has been virtually eliminated so that over 200W can be dissipated for durations in excess of one second at voltages up to 200V. Saturation voltage at 10A is under 1.5V.

This unique combination of characteristics is achieved using ion implanted base ballasting.[1] The ballast is voltage modulated by depletion with collector-base bias to increase ballast resistance as voltage is increased. This insures adequate ballasting at high voltage where it is needed, while limiting ballast losses at low voltage.

Reliability is enhanced because hot-spotting is avoided. Therefore, thermal resistance remains low even at maximum voltage. Oxide-passivated junctions insure stability of the low leakage currents.

These transistors are expected to find applications in power amplifiers, regulators, disc head positioners, deflection-yoke drivers for CRT displays, or other places where the ability to withstand the simultaneous application of high voltage and high current is important. The frequency response is an added bonus, especially in stabilizing feedback circuits, improving transient response, or avoiding quiescent current runaway in class-B amplifiers at high frequencies. Significantly, the base ballast resistance effectively suppresses the parasitic oscillations usually encountered with fast transistors.

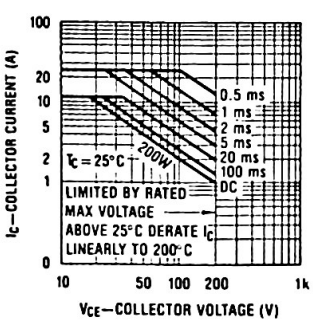
[1] R.J. Widlar, "Controlling Secondary Breakdown in Bipolar Power Transistors," National Semiconductor TP-16.

maximum ratings

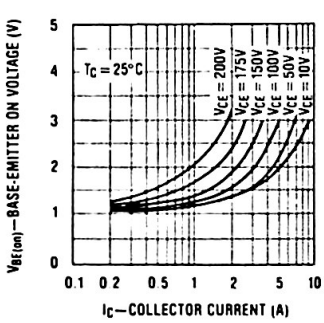
parameter		conditions	LT10-140V	LT10-200V
full power collecter voltage	$V_{CE(max)}$	$P_D \leq P_{D(max)}$, $T_J \leq 200°C$	140V	200V
emitter-base voltage	V_{EBO}	$I_C = 0$	5V	
collector current	I_C	continuous $t_{ON} \leq 5$ ms, $t_{OFF} \geq 50$ ms	12A 25A	
base current	I_B	continuous	5A	
dc power dissipation	$P_{D(max)}$	$V_{CE} \leq V_{MAX}$, $T_C \leq 25°C$	200W	
operating temperature range	T_J		−65°C to 200°C	
storage temperature range	T_{STG}		−65°C to 200°C	

typical characteristics

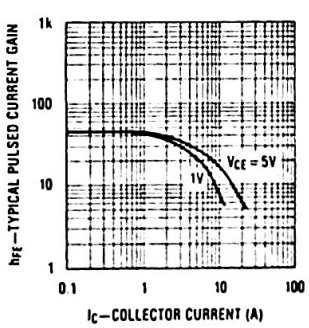
safe operating area



typical-base-emitter ON voltage vs collector current



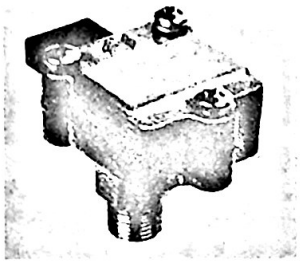
typical pulsed current gain vs collector current



IM-B25M101/Printed in U.S.A.

National Semiconductor

November 1981



LX18XXGBR Series Refrigerant Compatible Signal Conditioned Pressure Transducers

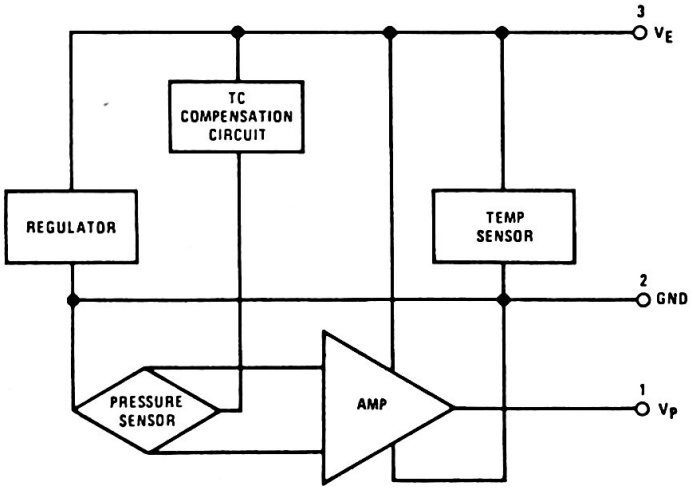
General Description

These are fully conditioned hybrid pressure transducers with temperature compensation and high level output voltage. The LX18XXGBR series transducers are provided in die cast zinc housings with 1/8" NPT fittings. They utilize special O-rings to provide freon compatibility[1]. Except for media compatibility, the LX18XXGBR series devices are functionally equivalent to the LX18XXGB series.

Features

- 0-100 psig and 0-300 psig
- High level output voltage, 2.5V to 12.5V
- Temperature compensated
- Freon compatibility
- Rugged zinc housings
- Field interchangeability
- Available from National distributors

Schematic Diagram



1—See Media Compatibility Section

IM-B25M111/Printed in U.S.A.

National Semiconductor

December 1981

MF10 Universal Monolithic Dual Switched Capacitor Filter

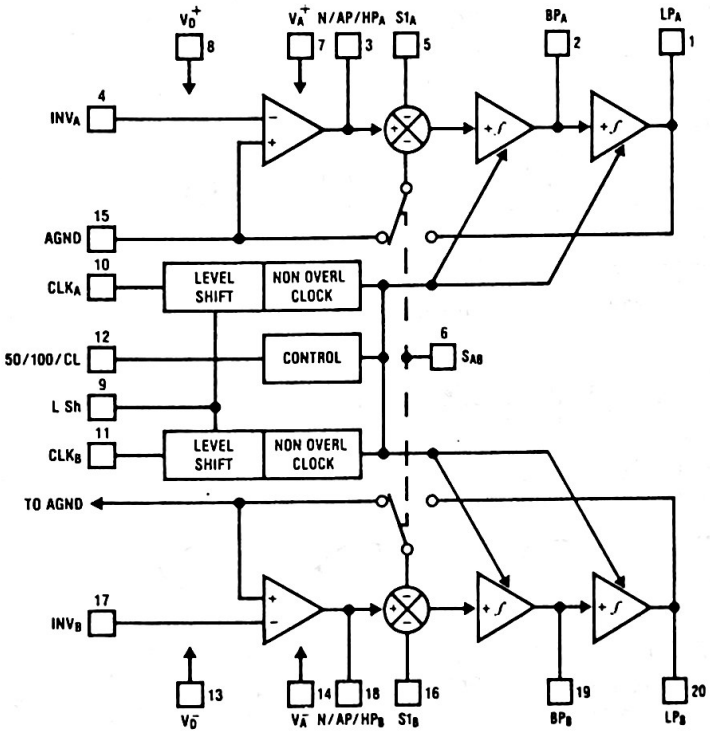
General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 20-pin 0.3" wide package
- Easy to use
- Clock to center frequency ratio accuracy = 0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_o \times Q$ range up to 200 kHz
- Operation up to 30 kHz

System Block Diagram



IM 825M121/Printed in U.S.A.

National Semiconductor

September 1981

MM74PC00 Quad 2-Input NAND Gate
MM74PC02 Quad 2-Input NOR Gate
MM74PC04 Hex Inverter
MM74PC08 Quad 2-Input AND Gate
MM74PC32 Quad 2-Input OR Gate

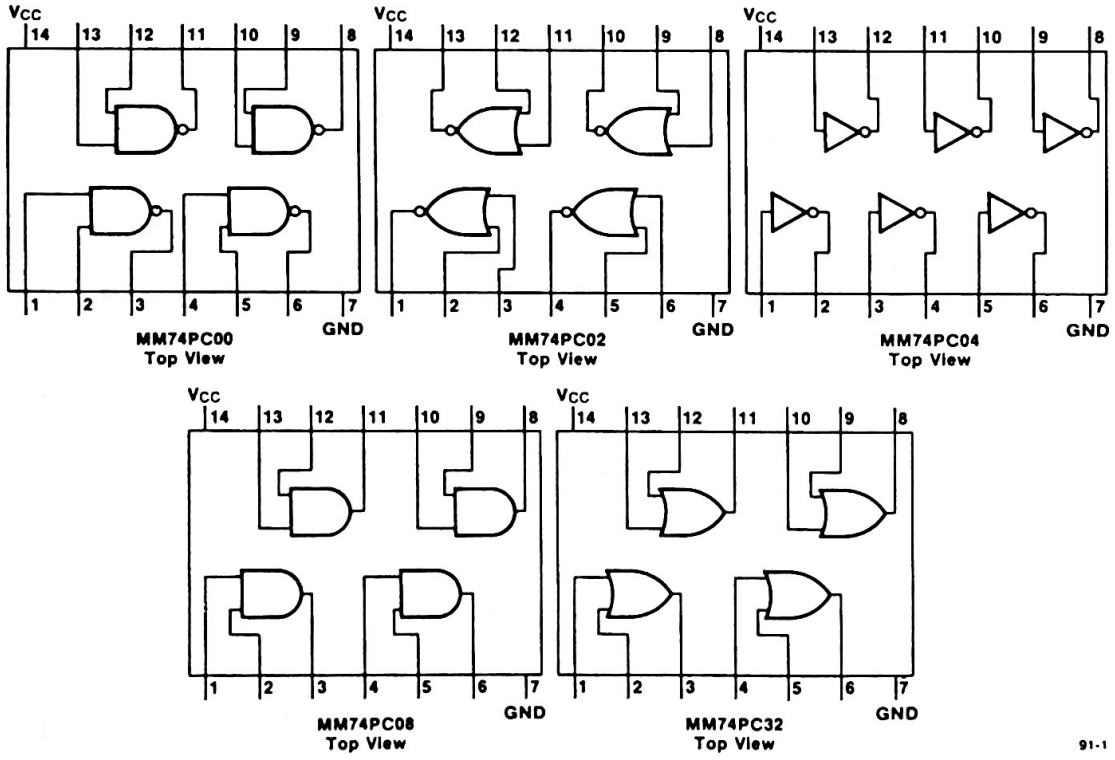
General Description

These Logic gates are fabricated using National's P²CMOS technology. This technology offers low power consumption, high noise immunity, and high speed. Function and pinout compatibility with Series-74 devices minimizes design time for those designers already familiar with the 74 logic family. These components may be utilized in completing NSC800 high-performance, low-power designs.

Features

- Single 5V Power Supply
- Low Power Dissipation
- Drive Capability of 100pF Load
- Fully Compatible with CMOS Logic Levels
- TTL Drive Capability
  When V_{CC} = 5V
- Fast: Typical Propagation Delay
  20ns (V_{CC} = 5V, C_L = 100pF)

Connection Diagrams



91-1

MM74PC00 Quad 2-Input NAND Gate; MM74PC02 Quad 1-Input NOR Gate; MM74PC04 Hex Inverter; MM74PC08 Quad 2-Input AND Gate; MM74PC32 Quad 2-Input OR Gate

In-H/B5M091/Printed in U.S.A.

National Semiconductor

July 1981

MM74PC74 Dual D Flip-Flop

General Description

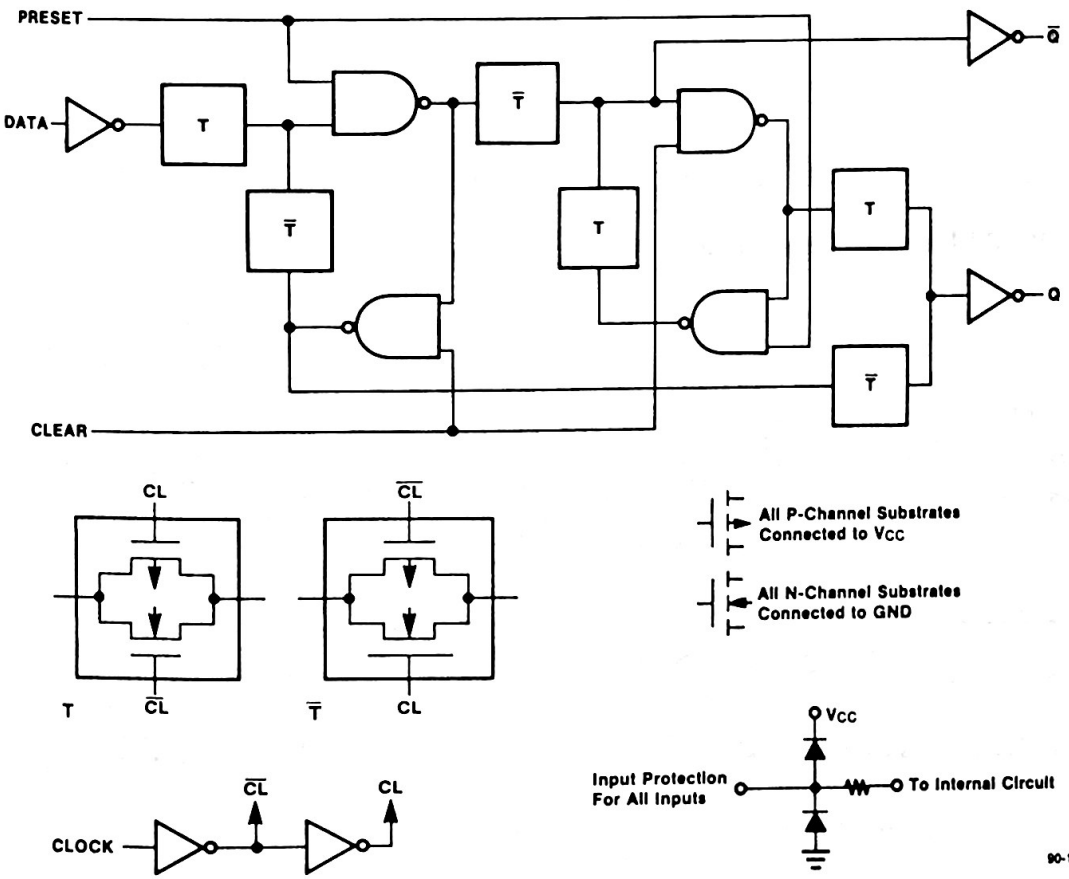
The MM74PC74 Dual D Flip-Flop (edge triggered) is fabricated using National's P²CMOS technology. This technology offers low power consumption, high noise immunity, and high speed. Function and pinout compatibility with Series-74 devices minimizes design time for those designers already familiar with the 74 logic family. The MM74PC74 may be utilized in completing NSC800 high-performance, low-power designs.

Each flip-flop has independent data, preset, clear and clock inputs, plus Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the rising edge of the clock pulse. Preset or clear status is independent of the clock and is caused by a low level at the preset, or clear input.

Features

- Single 5V Power Supply
- Typical Propagation Delay from Clock of 40ns (@5V)
- Low Power Dissipation
- Drive Capability of 100pF Load
- Fully Compatible with CMOS Logic Levels
- TTL Drive Capability
  When Vcc = 5V

Logic Diagram



In-H/B5M071/Printed in U.S.A.

National Semiconductor

July 1981

MM74PC138 3-Line to 8-Line Decoder/Demultiplexer

General Description

The MM74PC138 is fabricated using National's P2CMOS technology, which offers low power consumption, high noise immunity, and high speed. The speed of the MM74PC138 compares favorably with the speed of low power Schottky. Function and pinout compatibility with the 74LS138 and the 8205 minimizes design time for those designers already familiar with these two devices.

Three enable inputs are provided (two active low and one active high) to reduce the need for external gates or inverters when expanding a system.

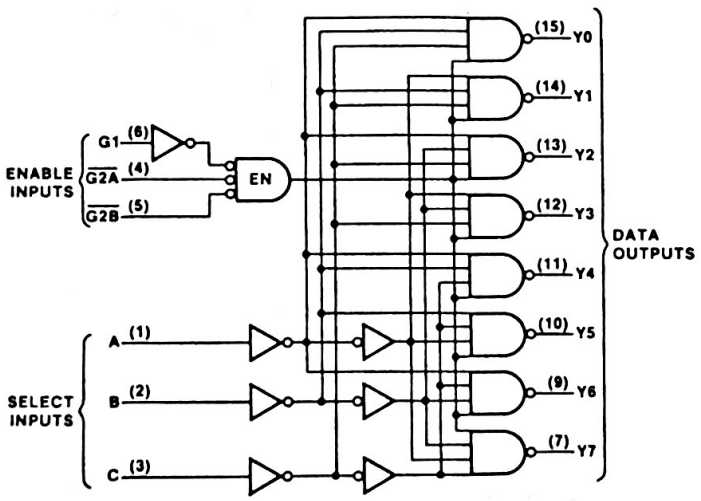
The MM74PC138's simple expansion in decoder and demultiplexer applications is particularly useful in completing NSC800 high-performance, low-power designs, while reducing component count.

When using the device as a demultiplexer, one of the three enable inputs (G1, G2A, G2B) serves as the data input terminal while the remaining enable inputs are enabled. The information will then be transmitted to the selected output, as determined by the 3-Line select address (A, B, C).

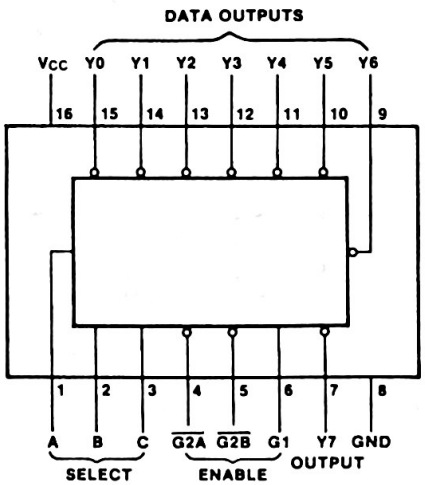
Features

- Simple Expansion - Three Enable Inputs
- P2CMOS Technology
- High Density 16-Pin Package
- Outputs Sink 6mA Minimum
- Single 5V Power Supply.
- High Noise Immunity: 0.45 V_{CC} Typical
- Low Quiescent Power Dissipation
- Full Interface to CMOS Logic Levels
- TTL Drive Capability
  When V_{CC} = 5V

MM74PC138 Decoder/Demultiplexer



Logic Diagram 93-1



Connection Diagram 93-2

In-H/B5M071/Printed in U.S.A.

National Semiconductor

July 1981

MM82PC08 8-Bit Bidirectional Transceiver

General Description

The MM82PC08 is an 8-bit TRI-STATE® high-performance, low-power P²CMOS transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured.

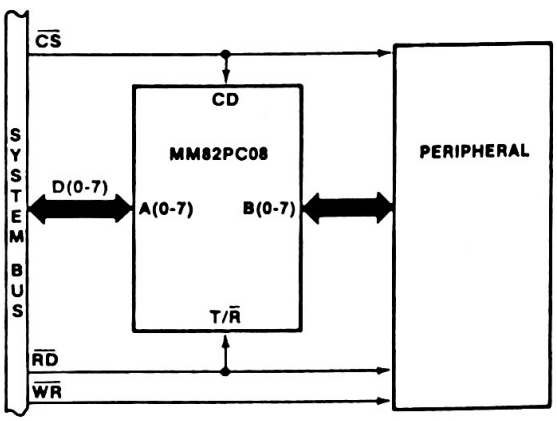
One input, Transmit/Receive, determines the direction of logic signals through the bidirectional transceiver. Transmit specifies data flow from Port A to Port B. Receive specifies data flow from Port B to Port A. The Chip Disable input disables both ports by placing them in the high-impedance state.

The MM82PC08 may be utilized in completing NSC800 high-performance, low-power designs.

Features

- P²CMOS Technology
- 8-Bit Bidirectional Data Flow Reduces System Package Count
- Bidirectional TRI-STATE Inputs/Outputs Interface with Bus-Oriented Systems
- Full Interface to CMOS Logic Levels
- Pinouts Simplify System Interconnections
- Transmit/Receive and Chip Disable Simplify Control Logic
- Compact 20-Pin Dual-In-Line Package
- Low Power
- Both Ports Have 100pF Load Drive Capability
- TTL Drive Capability When V_{CC} = 5V

MM82PC08 Basic System Configuration



89-1

In-H/B5M071/Printed in U.S.A.

National Semiconductor

SEPTEMBER 1981

MM5462, MM5463 Dual Alarm Digital Clock

General Description

The MM5462, M5463 digital dual alarm clock radio chips are monolithic MOS integrated circuits utilizing N-channel, low threshold, enhancement mode and ion-implanted depletion mode devices.

Each circuit contains all the logic necessary for a digital clock with sleep, dual alarm control, and is intended for clock-radio applications.

Real time and alarm time are displayed in hours-minutes and sleep time is displayed in minutes when setting the sleep counter.

An alarm output is provided that "beeps" a 60% duty cycle 700 Hz signal gated at a 2 Hz rate when either Alarm 1 Set time or Alarm 2 Set time matches the real time. A sleep output that provides a D.C. level is used to control the radio. It is activated with the alarm output or programmed via the sleep counter to turn off from 0 to 59 minutes after the sleep counter is set.

A snooze feature is provided for a 9 minute recurrence of the alarm after it has sounded.

Setting is done via the standard fast and slow Set buttons when in the Time Set, Alarm 1 Set, Alarm 2 Set or Sleep Set modes. These control inputs are TRI-STATE® inputs to reduce pin count.

The 50/60 Hz clock selects what segment data is on the outputs, i.e., a duplex LED display interface.

TRI-STATE is a registered trademark of National Semiconductor Corp.

The MM5462, MM5463 are bonded in 24-pin packages. The MM5462 has a 12-hour/50 Hz or a 12-hour/60 Hz option and the MM5463 has a 24-hour/50 Hz option.

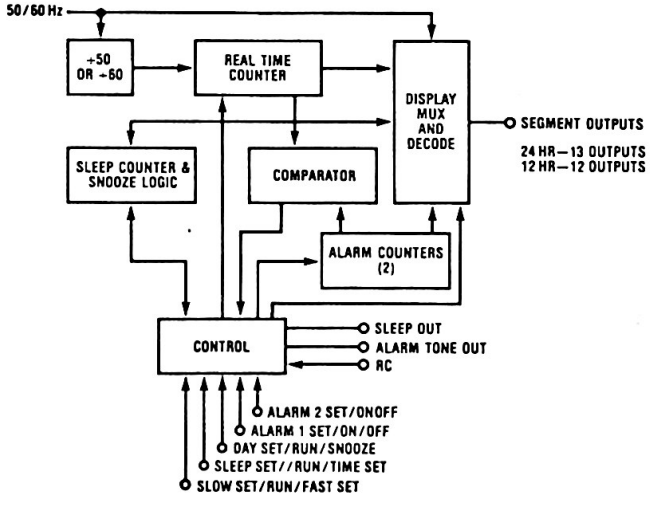
Features

- Duplex LED display drive
- Two 24-hour alarms
- Fast/slow set capability
- "Snooze" function (9 minutes)
- On-chip alarm oscillator
- Alarm tone output gated at 2 Hz rate
- Power fail indication — entire display flashes at a 1 Hz rate
- Automatic power-on reset
- PM display indicator
- Presettable 59 minute sleep timer

Applications

- Dual alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Industrial clocks
- Portable clocks
- Timers

Block Diagram



DA-B25M91/Printed in U.S.A.

National Semiconductor

November 1981

MM54240 Asynchronous Receiver/Transmitter Remote Controller

General Description

The MM54240 is a monolithic MOS integrated circuit utilizing N-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. The circuit is designed for processor-type remote control applications. The data transmission consists of a pulse width modulated serial data stream of 18 bits. This stream consists of 7 address bits, 1 command bit, 8 data bits, 1 parity bit and 1 dummy bit in that order.

The MM54240 can be operated in two modes, namely "master" and "slave". The master interfaces to a processor bus, and is capable of polling and controlling 128 slave circuits. The slave circuits are interfaced to remote data sources and/or data destinations.

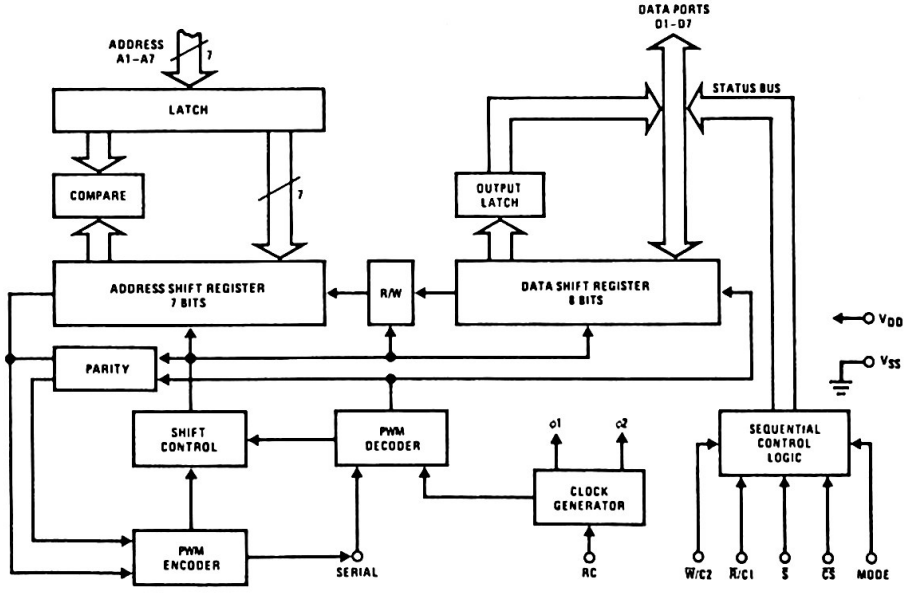
Applications

The MM54240 finds application in transmitting data to and receiving data from remote A-D/D-A, remote microprocessor units, remote digital transducer or remote data peripheral devices.

Features

- Supply voltage range — 4.75V to 11.5V single supply
- Low quiescent current — 5.0 mA maximum
- On-chip oscillator based on inexpensive R-C components
- Pulse width modulation techniques minimize error and maximize frequency tolerance
- Mode input for either master or slave operations
- Chip select ($\overline{CS}$) input in the master mode
- Selectable output port options in the slave mode
- Transmit/receive control output ($\overline{CS}$) in the slave mode

Functional Block Diagram



Pin Configuration

1	V_{SS}
2	D7 (MSB)
3	D6
4	D5
5	D4
6	D3
7	D2
8	D1
9	D0 (LSB)
10	Serial
11	Mode
12	$\overline{CS}$
13	V_{DD}
14	$\overline{R}$/C1
15	$\overline{W}$/C2
16	$\overline{S}$
17	OSC
18	A6 (MSB)
19	A5
20	A4
21	A3
22	A2
23	A1
24	A0 (LSB)

IM B25M111/Printed in U.S.A.

National Semiconductor

July 1979

MM58167 Microprocessor (MICROBUS™) Compatible Real Time Clock

General Description

The MM58167 is a low threshold metal-gate CMOS circuit that functions as a real time clock calendar in bus-oriented microprocessor systems. The device includes an addressable counter, addressable latch for alarm-type functions, and 2 interrupt outputs. A power-down input allows the chip to be disabled from the outside world for standby low power operation. The time base is generated from a 32,768 Hz crystal-controlled oscillator.

Features

- MICROBUS™ compatible
- Thousandths of seconds, hundredths of seconds, tenths of seconds, seconds, minutes, hours, day of the week, day of the month, and month counters with corresponding latches for alarm-type functions
- Interrupt output (maskable) with 8 possible interrupt signals:
  - Latch and counter comparison
  - Every tenth of a second
  - Every second
  - Every minute
  - Every hour
  - Every day
  - Every week
  - Every month
- Power-down mode that disables all outputs except for an interrupt output that occurs on a counter latch comparison. This is not the same as the maskable interrupt output
- Don't care states in the latches
- Status bit to indicate clock rollover during a read
- 32,768 Hz crystal reference, with only the input tuning capacitor and load capacitor needed externally
- Four year calendar

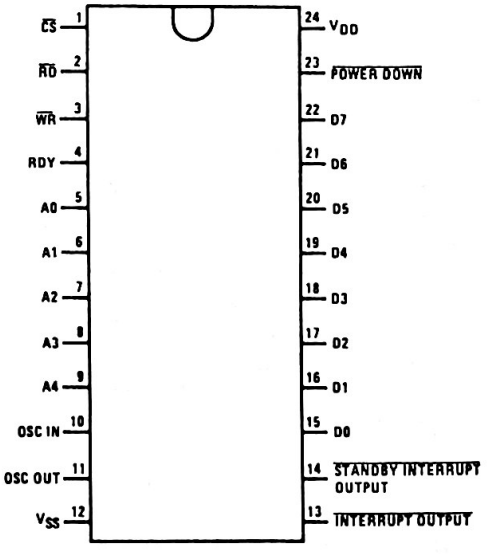
Functional Description

The MM58167 is a microprocessor oriented real time clock. The circuit includes addressable real time counters and addressable latches, each for thousandths of seconds through months. The counter and latch are divided into bytes of 4 bits each. When addressed, 2 bytes will appear on the data I/O bus. The data, in binary coded decimal, can be transferred to and from the counters via the data I/O bus so that each set of 2 bytes (1 word) can be accessed independently as grouped in Table I.

If either of the bytes in the above 8-bit counter words do not legally reach 4-bit lengths (e.g., day of the week uses only the 3 least significant bits) the unused bits will be unrecognized during a write and held at V_{SS} during a read. If any illegal data is entered into the counters during a write cycle, it may take up to 4 clocks (4 months in the case of the month counter) to restore legal BCD data to the counter. The latches will read and write all 4 bits per byte. Each of the counter and latch words can be reset with the appropriate address and data inputs. The counter reset is a write function. The latches can be programmed to compare with the counters at all times by writing 1's into the 2 most significant bits of each latch, thus establishing a don't care state in the latch. The don't care state is programmable on the byte level, i.e., tens of hours can contain a don't care state, yet unit hours can contain a valid code necessary for a comparison.

Connection Diagram

Dual-In-Line Package



TOP VIEW

National Semiconductor

August 1981
PRELIMINARY

NMC27C16 16,384-Bit (2048 x 8) UV Erasable CMOS PROM

Parameter/Part Number	NMC27C16Q-45	NMC27C16Q-55	NMC27C16Q-65
Access Time (ns)	450	550	650
Active Current (mA @ 1 MHz)	25	25	25
Standby Current (μA)	100	100	100

General Description

The NMC27C16 is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

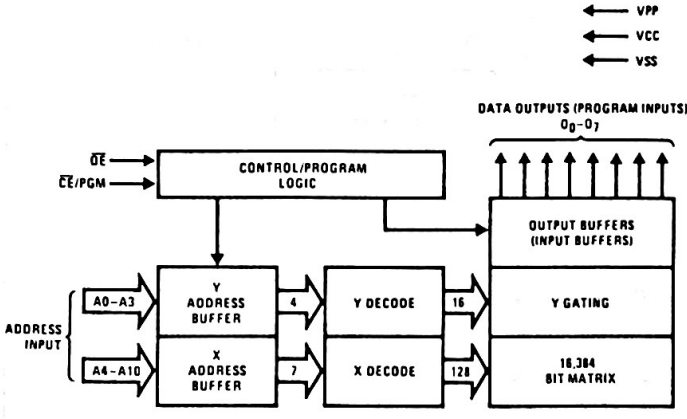
The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, P^2CMOS silicon gate technology.

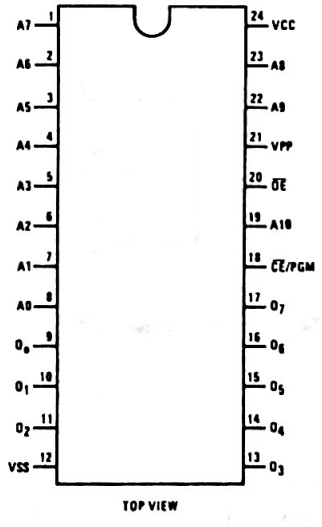
Features

- CMOS power consumption
- Performance compatible to NSC800 CMOS microprocessor and NMC6716 synchronous CMOS EPROM
- 2048 x 8 organization
- Pin compatible to 2716
- Access time down to 450 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Pin Connection During Read or Program

Mode	Pin Name/Number				
	CE/PGM 18	OE 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0-A10	Address Inputs
O_0-O_7	Data Outputs
CE/PGM	Chip Enable/Program
OE	Output Enable
VPP	Read 5V, Program 25V
VCC	5V
VSS	Ground

TRI-STATE® is a registered trademark of National Semiconductor Corp.

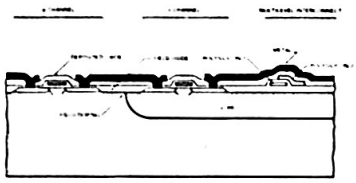
IM-B25M81/Printed in U.S.A.

NMC27C16 16,384-Bit (2048 x 8) UV Erasable CMOS PROM

National Semiconductor

December 1981

NS80C48/80C35 P²CMOS™ Microcomputer/Microprocessor Family



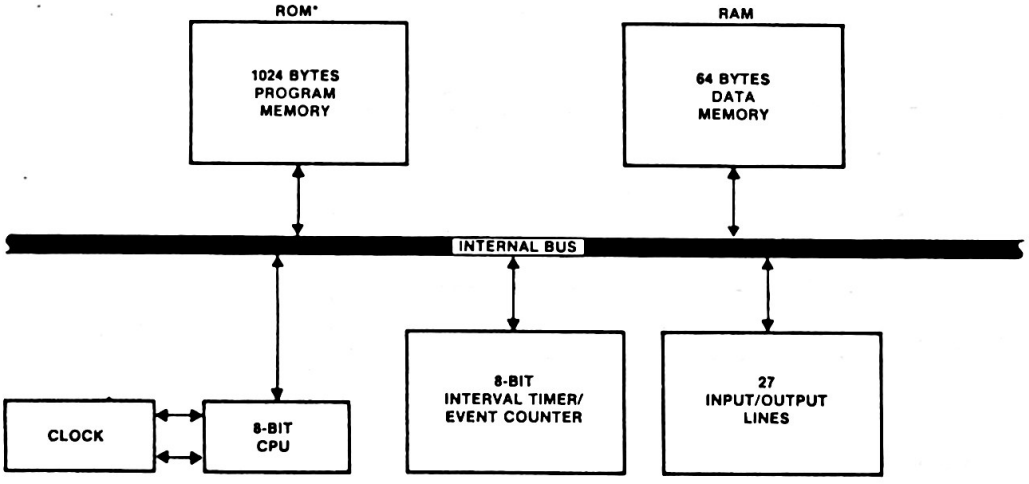
General Description

The NS80C48 is a parallel 8-bit microcomputer contained in a standard 40-pin, dual-in-line package. The device is fabricated using P²CMOS silicon gate technology. This technology provides the system designer with devices that equal the speed performance levels of comparable NMOS products, combined with low-power advantages of CMOS. The NS80C48 is a stand-alone microcomputer designed for efficient controller applications. It executes powerful bit manipulative instructions and BCD as well as binary arithmetic. The NS80C48 contains on-chip oscillator and clock circuits, 1K x 8 ROM program memory, 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit Timer/Counter. Also, it is pin and instruction compatible with the XMOS™ INS8048.

Features

- 8-Bit CPU, RAM, ROM, I/O in a Single Package
- 2.5 μsec Cycle Time, 6MHz Oscillator
- Low Power
- Very Low Stand-by Power
- Expandable Memory and I/O
- Single-Level Interrupt
- Efficient Instructions
- Instruction Compatible to INS8048
- Pin Compatible to INS8048

NS80C48/NS80C35 Block Diagram



*Not Applicable to INS80C35

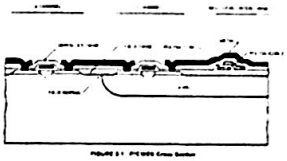
31-1

In-H/B30M121/Printed in U.S.A.

National Semiconductor

October 1981

NS80CX48/80CX35 P²CMOS™ Microcomputer/ Microprocessor Family



General Description

The NS80CX48 is a parallel 8-bit microcomputer contained in a standard 40-pin, dual-in-line package. The device is fabricated using P²CMOS silicon gate technology. This technology provides the system designer with devices that equal the speed performance levels of comparable NMOS products, combined with low-power advantages of CMOS. The NS80CX48 is a stand-alone microcomputer designed for efficient controller applications. It executes powerful bit manipulative instructions and BCD as well as binary arithmetic. The NS80CX48 contains on-chip oscillator and clock circuits, 1K x 8 ROM program memory, 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit Timer/Counter. Also, it is pin and instruction compatible with the XMOS™ INS8048.

The NS80CX48 has an extra feature mode which permits enhanced microcomputer performance. When the NS80CX48 is not in the extra feature mode, the device operates the same as the standard INS8048. Device capabilities can be expanded using readily available compatible components. The NS80CX35 is a ROMless version of the NS80CX48.

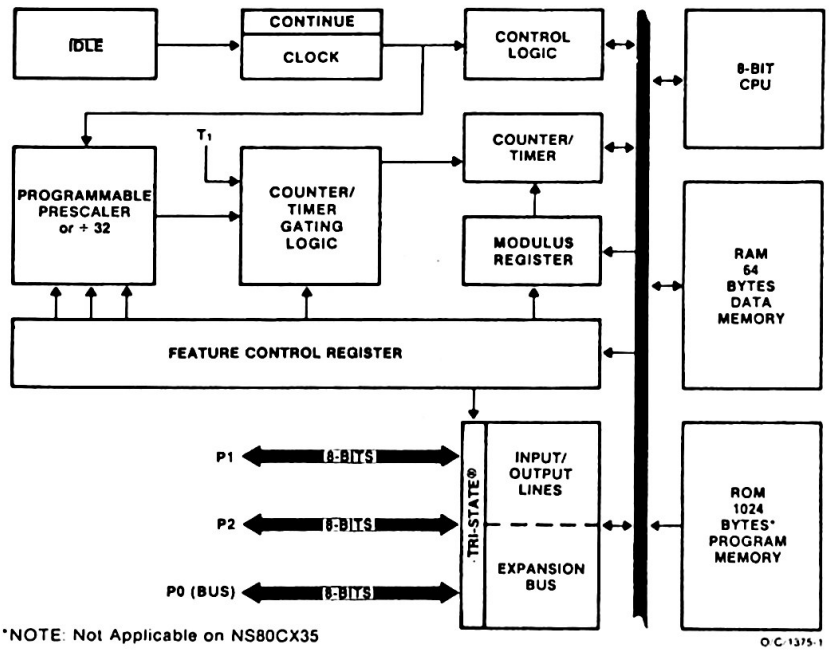
Features — NS80CX48

- 8-Bit CPU, RAM, ROM, I/O in a Single Package
- 2.5 μsec Cycle Time, 6MHz Oscillator
- Low Power
- Very Low Stand-by Power
- Expandable Memory and I/O
- Single-Level Interrupt
- Efficient Instructions
- Instruction Compatible to INS8048
- Pin Compatible to INS8048

Extra Features

- Programmable Prescaler for Timer/Counter
- Gating Mode for Timer/Counter
- Modulo Mode for Timer/Counter
- Power Down Mode (Idle Mode)

NS80CX48/NS80CX35 Block Diagram



*NOTE: Not Applicable on NS80CX35

OC/1375-1

In-H-B30M111/Printed in U.S.A.

National Semiconductor

September 1981

NS87P50 Piggy-Back Microcomputer

General Description

The NS87P50 Piggy-Back 8-bit microcomputer is a prototyping aid for INS8048, 8049 and 8050 designs. It is fabricated using National's scaled N-channel, silicon gate MOS process, XMOS. Housed in a 40-pin dual-in-line package, the NS87P50 includes a plug-in adapter that accepts two additional packages: 1) A 24-pin EPROM, 2758A, 2716 or 2732, which replaces the normally on-board ROM of the INS8048 series. 2) A program module to select either the INS8048 or 8049 microcomputer. The INS8050 microcomputer is selected when no module is used.

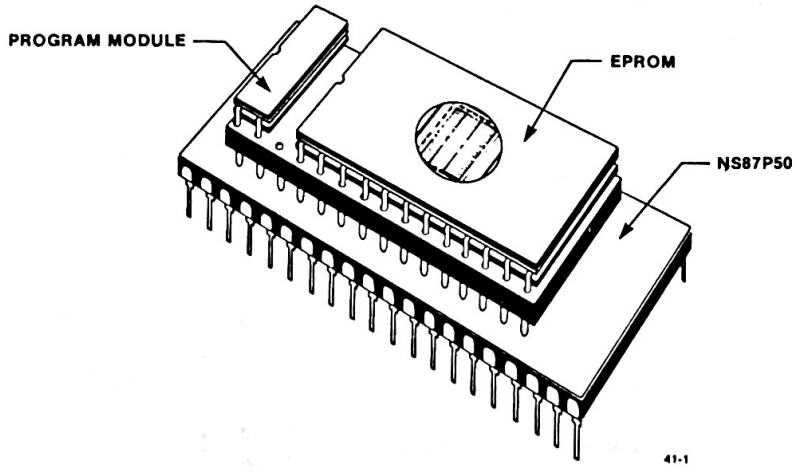
Architecture	RAM Array	EPROM/Array
INS8048	64 x 8	2758A/1K x 8
INS8049	128 x 8	2716/2K x 8
INS8050	256 x 8	2732/4K x 8

The Piggy-Back microcomputer contains the system timing, control logic, RAM data memory, EPROM socket and program module interface, plus 27 I/O lines to implement prototype program development and emulation. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory is derived from an instruction set comprised of predominantly single byte instructions, the remaining instructions are two bytes in length.

Features

- Emulates the INS8048, 8049 and 8050
- 8-Bit CPU, RAM, I/O In Single Package
- Plug In Adapter for EPROM and Program Module
- 2.5μsec Cycle, 6 MHz Clock; 1.36μsec Cycle, 11 MHz Clock
- On-Chip Oscillator and Clock (Or External Source)
- 27 I/O Lines
- Expandable Memory and I/O
- 8-Bit Timer/Counter
- Single Level Interrupt
- 96 Instructions
- Binary and BCD Arithmetic
- Single +5V Power Supply
- Low Standby Power
- Low Voltage Standby 3 6V Minimum

Piggy-Back Package



S-B-5M 091/Printed in U.S.A.

National Semiconductor

July 1981

NSC800 High-Performance Low-Power Microprocessor

General Description

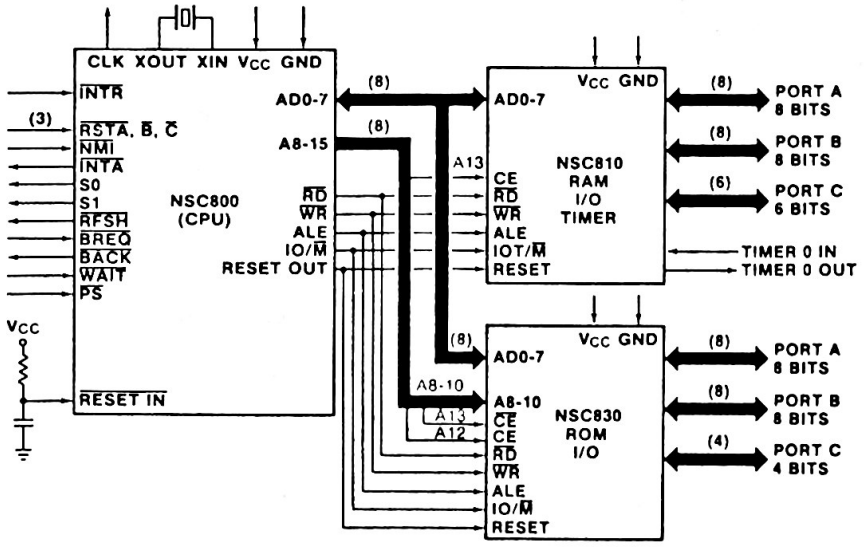
The NSC800 is an 8-bit microprocessor that functions as the central processing unit (CPU) in National Semiconductor's NSC800 microcomputer family. The device is fabricated using National's P²CMOS technology. This technology provides the system designer with devices that equal the performance levels of comparable NMOS products, combined with the low-power advantages of CMOS. Many system functions are incorporated on the device, such as: vectored priority interrupts, refresh control, power-save feature and interrupt acknowledge. The NSC800 is housed in a 40 pin, dual-in-line package.

Dedicated memories (NSC810 RAM-I/O Timer and NSC830 ROM-I/O) have on-chip logic for direct interface to the NSC800. In addition, National also offers a full line of P²CMOS and CMOS components to allow a full low-power solution to system designs.

Features

- Single 5V Power Supply
- Fully Compatible with Z80™ Instruction Set
- Powerful Set of 158 Instructions
- 10 Addressing Modes
- 22 Internal Registers
- Low Power, 50mW at 5V V_{CC}
- Multiplexed Bus Structure
- On-Chip Bus Controller and Clock Generator
- On-Chip 8-Bit Dynamic RAM Refresh Circuitry
- Speed: 1.6 μs Instruction Cycle at 2.5 MHz; NSC800-2 2 MHz; NSC800-1 1 MHz
- Fast Version (NSC800A): 1 μs Instruction Cycle at 4 MHz (Availability to be Announced)
- Capable of Addressing 64K Bytes of Memory and 256 I/O devices
- Five Interrupt Request Lines On-Chip
- Schmitt Trigger Input on Reset
- Unique Standby-Current (Power Save) Feature

NSC800 Microcomputer Family Block Diagram



  In-H B5M071 Printed in U.S.A.

National Semiconductor

Preliminary

NSC810 RAM-I/O-Timer

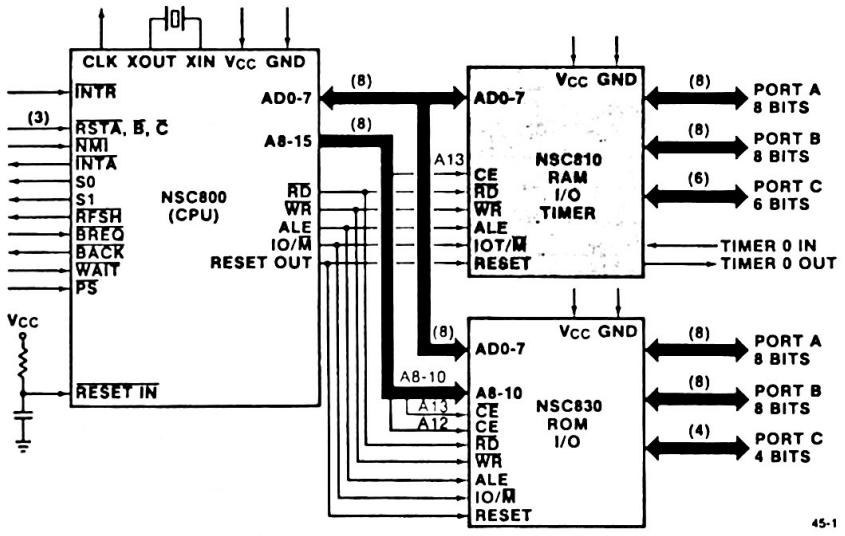
General Description

The NSC810 is a RAM-I/O-Timer device contained in a standard 40-pin, dual-in-line package. The chip, which is fabricated using P²CMOS silicon gate technology, functions as a memory, an input/output peripheral interface and a timing device. The memory is comprised of 1024 bits of static RAM organized as 128 x 8. The I/O portion consists of 22 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written or read in bytes. Several types of strobed mode operations are available through Port A. The timer portion of the device consists of two programmable 16-bit binary down-counters each capable of operation in any one of six modes. Timer counts are extendable by one of the available prescale values.

Features

- 128 x 8 Random Access Memory
- Three Programmable I/O Ports
- Two 16-Bit Programmable Counter/Timers
- 3-12 V Power Supply
- Very Low Power Consumption
- Fully Static Operation
- Single-Instruction I/O Bit Operations
- Timer Operation — DC to 4MHz
- Directly Compatible with NSC800 Family

NSC800 Microcomputer Family Block Diagram



Printed in U.S.A.

National Semiconductor

July 1981

NSC830 ROM-I/O; NSC831 I/O Only

General Description

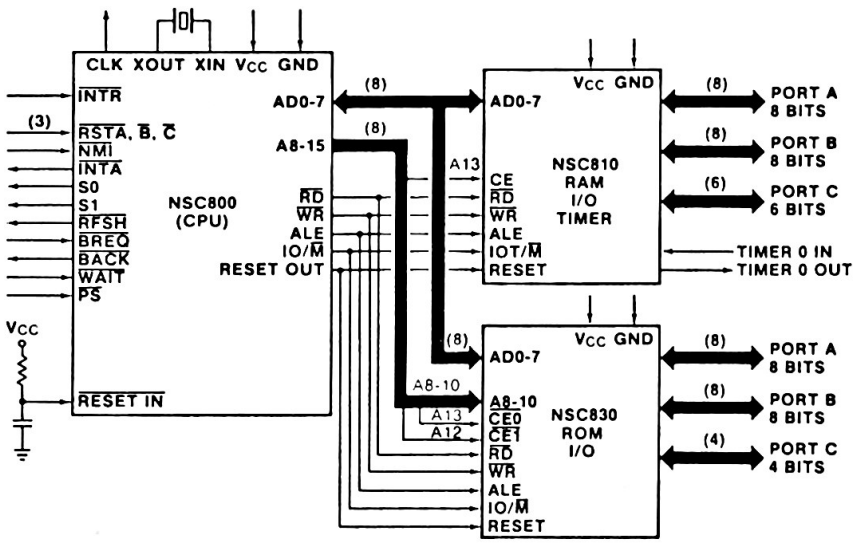
The NSC830 is a ROM-I/O device contained in a standard 40-pin, dual-in-line package. The chip, which is fabricated using P^2CMOS silicon gate technology, functions as a memory, and an input/output peripheral interface device. The memory is comprised of 16,384 bits of ROM organized as 2048 x 8. The I/O portion consists of 20 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written to or read from in bytes. Several types of strobed mode operations are available through Port A.

The NSC831 I/O Only is similar to the NSC830 except it has no ROM. The NSC831 is useful for prototyping work prior to ordering the NSC830, and when on-chip ROM is not required.

Features

- 2K x 8 Read Only Memory
- Three Programmable I/O Ports
- Single 5V Power Supply
- Very Low Power Consumption
- Fully Static Operation
- Single-Instruction I/O Bit Operations
- Directly Compatible with NSC800 Family
- Strobed Modes Available on Port A

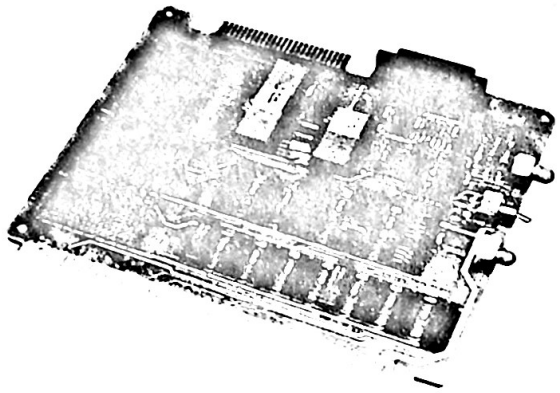
NSC800 Microcomputer Family Block Diagram



In-H B5M071 Printed in U.S.A.

NSC888

NSC800 Evaluation Board



Features

- NSC800 8-Bit P²CMOS™ CPU
- Executes Z80™ Instruction Set
- 20 Programmable Parallel I/O Lines
- Two 16-Bit Programmable Counters/Timers
- Powerful 2K x 8 Monitor Program
- Five Levels of Vectored Prioritized Interrupts
- RS232 Interface
- 1K x 8 P²CMOS RAM with Sockets for Up to 4K x 8 RAM
- Socket for additional 2K x 8, 2716 Compatible Memory Component
- Wire Wrap Area
- Edge Connectors for System Expansion
- Single-Step Operation Mode
- Fully Assembled and Tested

Product Overview

The NSC888 is a self-contained microprocessor board which enables the user to quickly evaluate the performance and features of the NSC800 product family. This fully assembled, tested board requires only the addition of a +5V supply and an RS232 interface cable to the users terminal to begin NSC800 evaluation.

A powerful system monitor is provided on the board which controls serial communications via the RS232 port. The monitor also includes command functions to load, execute and debug NSC800 programs.

The board includes an NSC800 CPU plus RAM, EPROM, I/O, Timers and interface components yet draws only 30mA from the +5V supply and 3mA from the -5V supply.

Although designed primarily as an assessment vehicle, the NSC888 can be readily programmed and adapted to a variety of uses. Wire wrap area is provided on-board for the user to build up additional circuitry or interfaces, thus tailoring this high-performance, low-power microprocessor board to meet individual needs.

P²CMOS is a trademark of National Semiconductor Corp.

Z80 is a trademark of Zilog Corp.

National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, California 95051 408 737-5000

Circle DATA UPDATE No. 950514

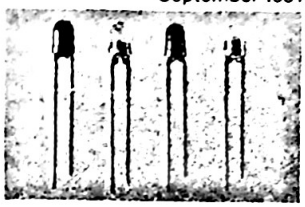
Printed in U.S.A.

National Semiconductor

September 1981

NSL5080 Series T-1 Size LED Lamps

NSL5080 Uncolored Transparent-Lens
NSL5081 Uncolored Diffused-Lens
NSL5082 Red Transparent-Lens
NSL5086 Red Diffused-Lens
NSL5286 Green Diffused-Lens
NSL5386 Yellow Diffused-Lens
NSL5786 Hi-Intensity Red Diffused-Lens



General Description

The T-1 size (0.125" dia) series lamps are solid state LEDs encapsulated in a plastic package. The lens configuration is designed for applications where space is a premium. High axial luminous intensity with a wide viewing angle and good ON-OFF contrast characterize these small lamps.

Applications

- Appliances
- Cameras
- Computers
- Indicator lamps
- Pilot lamps
- Circuit status
- Mobile and portable equipment
- High density arrays
- Vending machines
- Test equipment
- Medical instruments

Features

- Wide viewing angle
- Wire wrap or solder leads
- IC compatible
- Reliable and rugged
- Low power consumption
- Long life
- Mount on 0.125" centers

Absolute Maximum Ratings

DC Forward Current	50 mA
Reverse Voltage	5.0V
Power Dissipation Derate Linearly 1.0 mW/°C above 25°C	100 mW
Peak Forward Current 1 μs Pulse, 300 pps	1A
Operating and Storage Temperature Range	−55°C to +100°C
85/85 Temperature—Humidity	1000 hrs
Lead Temperature (Soldering, 7 seconds)	230°C

Electrical and Optical Characteristics (25°C)

Parameter	Conditions	5080	5081	5082	5086	5286	5386	5786	Units
Forward Voltage (V_F)	*Figure 1*								
Typ	I_F = 20 mA	1.8	1.8	1.8	1.8				V
Max		2.0	2.0	2.0	2.0				
Typ	I_F = 10 mA					2.3	2.2	2.1	V
Max						3.0	3.0	3.0	
Reverse Breakdown Voltage (BV_R)									
Min	I_R = 100 μA	5.0	5.0	5.0	5.0	5.0	5.0	5.0	V
Light Intensity (I)	*Figure 2*								
Typ	I_F = 20 mA	1.2	2.4	1.2	2.4	3.0			mcd
Min		0.3	0.3	0.3	0.3	0.5			
Typ	I_F = 10 mA						4.0	2.5	mcd
Min							2.5	0.5	
Peak Wavelength									
Typ	I_F = 20 mA	660	660	660	660	565	585	635	nm
Spectral Width, Half-Intensity									
Typ	I_F = 20 mA	40	40	40	40	30	30	40	nm
Light Rise and Fall Time, 10%-90%									
Typ	50Ω System	50	50	50	50	50	50	50	ns
Angle of Half-Intensity Off Axis	*Figures 3 and 4*								
Typ	I_F = 20 mA	50	60	50	60	60	60	60	Degrees
Capacitance									
Typ	V = 0, 1 MHz	75	75	75	75	50	50	50	pF

IM-B25M91/Printed in U.S.A.

National Semiconductor

August 1981

NSM4005A LED Display with Driver

General Description

The NSM4005A is a 4-digit 0.5" height LED display with a serial data/parallel data-out LED driver designed to operate with minimal interface to the data source. Current drive to the LEDs is programmable by setting a reference current to a single pin.

Features

- Four 0.5" digits with right-hand decimal points
- LED current is programmable
- Serial data input
- Clock format—colon between center digits
- Enable
- TTL compatible
- Wide power supply operation
- Direct current drive (non-multiplexed)

Applications

- COPS™ or microprocessor display
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram

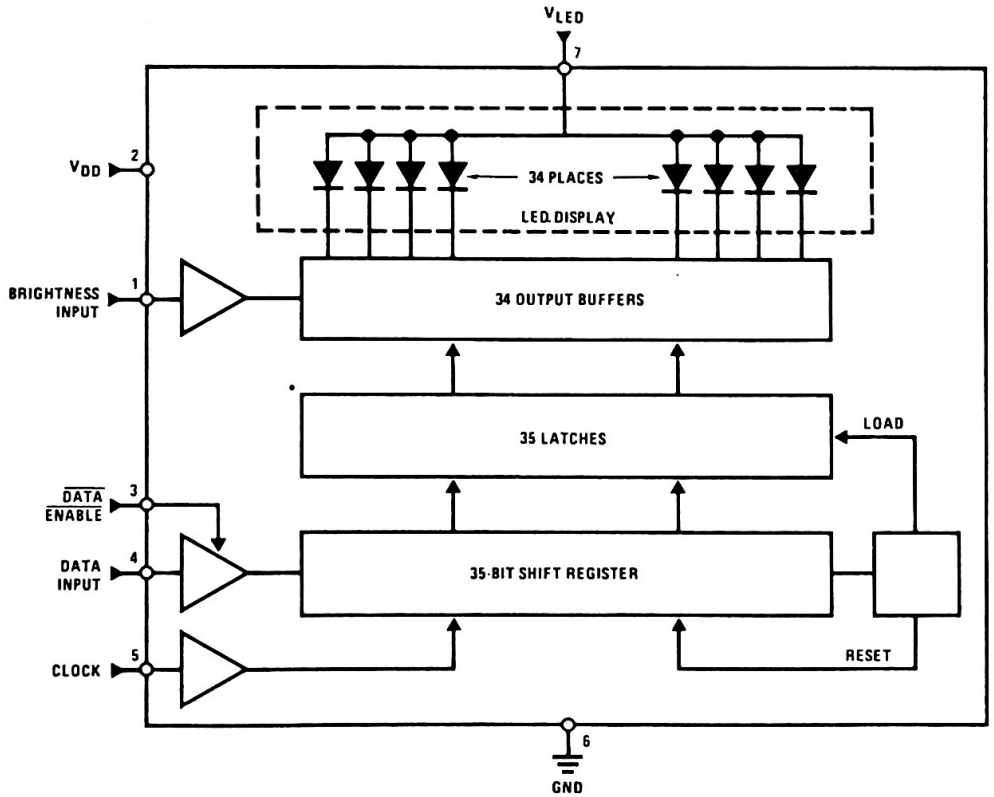


FIGURE 1

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IM-B25M81/Printed in U.S.A.

National Semiconductor

August 1981

NSM4307 LED Display with Driver

General Description

The NSM4307 is a 2-digit 0.3" height LED display with a serial data/parallel data-out LED driver designed to operate with minimal interface to the data source. Current drive to the LEDs is preset at approximately 10 mA per segment with an on-board resistor. LED supply voltage of 4.4V can be supplied by 5.0V minus an external dropping diode.

- Enable
- TTL compatible
- Direct current drive (non-multiplexed)

Features

- Two 0.3" digits
- Serial data input
- Single power supply (+5V) operation with external dropping diode

Applications

- COPS™ or microprocessor display
- Digital, thermometer, counter
- Instrumentation readouts
- Channel indicator

Block Diagram

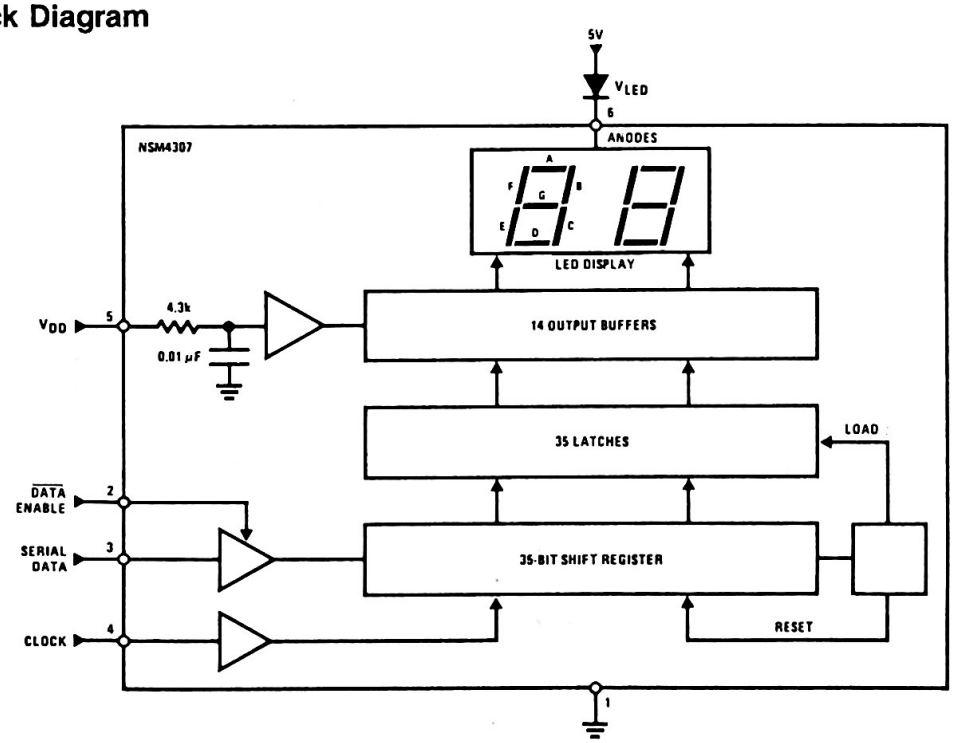

FIGURE 1

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IM-B25M81/Printed in U.S.A.

National Semiconductor

August 1981

NSM4507 LED Display with Driver

General Description

The NSM4507 is a 2-digit 0.5" height LED display with a serial data/parallel data-out LED driver designed to operate with minimal interface to the data source. Current drive to the LEDs is programmable by setting a reference current to a single pin.

- TTL compatible
- Wide power supply operation
- Direct current drive (non-multiplexed)

Features

- Two 0.5" digits
- LED current is programmable
- Serial data input
- Enable

Applications

- COPS™ or microprocessor display
- Thermometer, digital counter
- Instrumentation readouts
- Channel indicator

Block Diagram

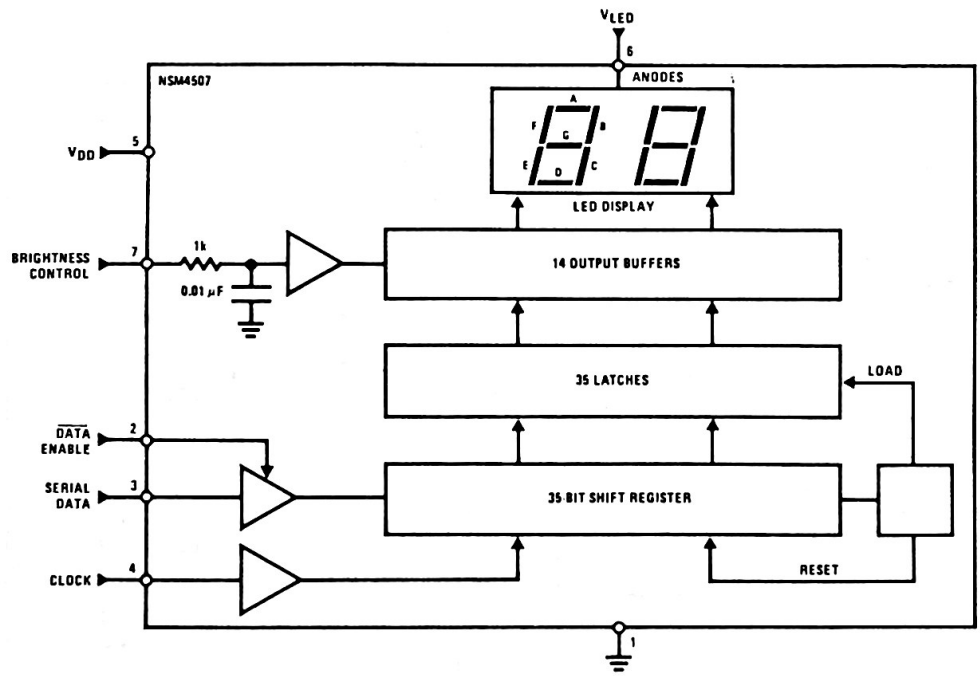

FIGURE 1

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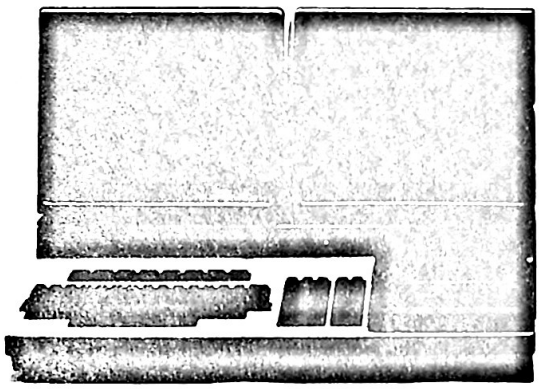
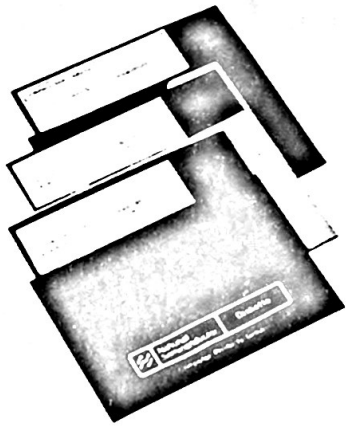
IM-B25M81/Printed in U.S.A.

PALASM™ Software Program





- **STARPLEX™ and STARPLEX II™ compatible**
- **Program generation for National PAL™ devices**
- **Compatible with National's Universal PROM Programmer Interface**

Product Description

Like PROM, the Program-Array-Logic (PAL) device has a single array of fusible links. These links may be left intact or "blown" to create various combinations of AND and OR gates to peform the desired function.

Programming a PAL device may be done manually with the designer marking PAL logic diagrams with appropriate fuse interconnections or via PALASM, an automatic fuse pattern generator.

PALASM is a FORTRAN IV program which transforms PAL symbolic equations into a format compatible with standard PAL programming personality modules. The output of this program is formatted to create the proper fuse patterns in PAL devices.

The pins of a PAL devices are represented as symbolic names and equations are given to specify how the pins are to be connected. For example, P = Q*R indicates that P is the logical AND of pins Q and R. The PALASM program translates these symbolic equations into a fuse pattern, absolute format, hex format, BHLF and/or BPNF format.

PALASM is supported on both STARPLEX and STARPLEX II development systems, and is an integral part of the Universal PROM Programmer Interface.

Functional Description

PALASM uses three designated files for input/output. These files are:

1. Input file
2. ABSOLUTE file
3. Object file

The Input file is the user-defined data file, a series of Boolean expressions defining the input/output relationship for each pin of the PAL devices.

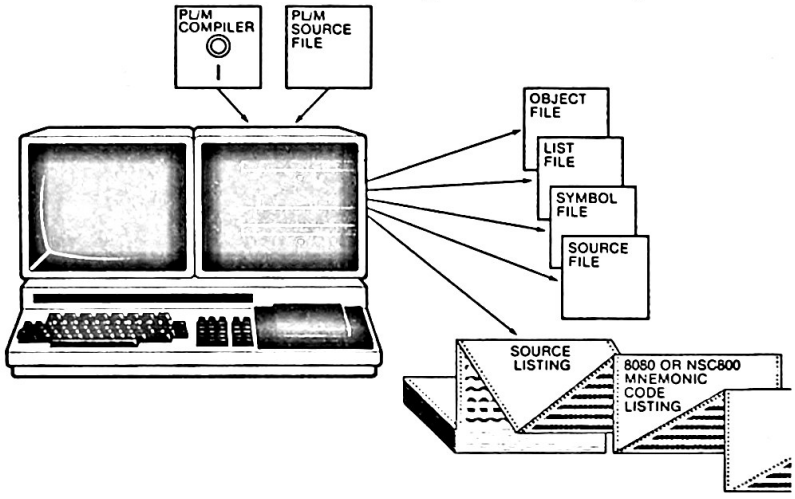
The Output file may be either an ABSOLUTE file for input to the standard PROM programmer or an object file in one of several formats. These optional formats are useful for verification of the plot, or for inputs to various PROM programmers not directly supported by STARPLEX.

Optional formats are:

A = ABSOLUTE
B = PLOT
H = HEX
S = SHORT HEX
L = BHLF HIGH LOW
N = BPNF POSITIVE-NEGATIVE
M = MAP

DA-B30M71/Printed in U.S.A.

PLM80
PL/M High Level Language Compiler for STARPLEX™ Development Systems



- **Executes on all STARPLEX/ STARPLEX II™ Development Systems**
- **Code generation for 8080/8085 and NSC800/Z80® microprocessors**
- **Relocatable and linkable object code output**
- **Reentrant procedures as specified by user**
- **Compatible with existing industry standard PL/M-80**
- **Hardware access via highlevel statements (interrupt systems, absolute addresses, and input/output ports)**

Product Description

PLM80 is a high level language compiler designed for STARPLEX and STARPLEX II Development Systems. Available in two versions, this highly efficient compiler generates relocatable object code for 8080/8085 and NSC800/Z80 microprocessors.

PL/M has proven to be one of the most popular, effective and powerful program development tools available. Programmer productivity and reliability are greatly improved because the programmer can concentrate on system development rather than all the details of assembly languages. Since PL/M uses data structures that are very close to typical microprocessor architectures, it allows for efficient use of the machine. PL/M programs are efficiently converted to assembly language instructions, thus requiring fewer statements. Software development and maintenance costs are significantly reduced.

Free form PL/M source programs are efficiently and effectively converted into 8080/8085 or NSC800/Z80 assembly language instructions. A given program, when written in PL/M, requires fewer statements than would the equivalent program written in assembly language. Thus, software development and maintenance costs are significantly reduced due to the problem oriented structure that results naturally from the use of PL/M. User programming conventions and structured programming techniques are easily accommodated by the free form source statements of PL/M.

Functional Description

The PLM80 Compiler is a STARPLEX System program which accepts STARPLEX PLM80 language source modules and produced linkable object modules. Object modules may be linked to form executable PLM80 programs. The PLM80 compiler is also designed to accept programs written in the industry standard PL/M programming language.

The STARPLEX PLM80 compiler invocation is similar to that of other STARPLEX software. The 8080 version of the compiler in particular has all the features of the existing industry standard PL/M-80

DA-B30M121/Printed in U.S.A.

National Semiconductor

December 1981

TP3020/TP3021 Monolithic CODECs

General Description

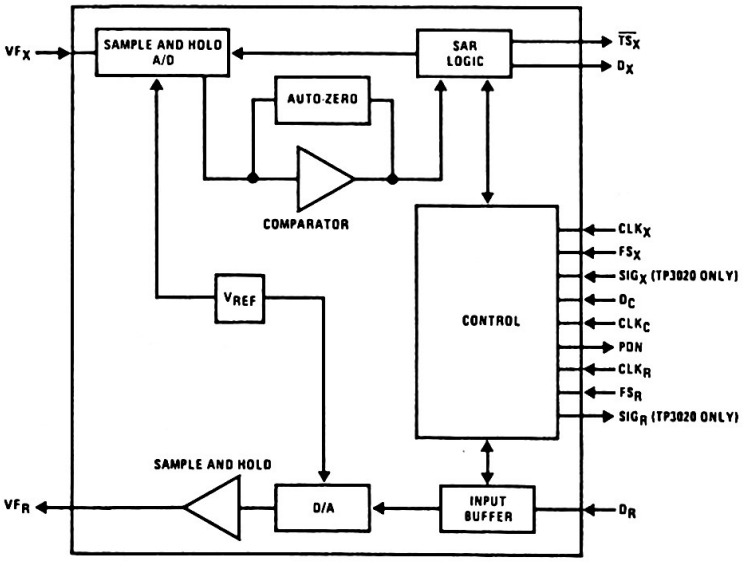
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



IM-B25M121/Printed in U.S.A.

National Semiconductor

December 1981

TP3040/TP3040A PCM Monolithic Filter

General Description

The TP3040/TP3040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Features

- Exceeds all D3/D4 and CCITT specifications
- +5V, −5V power supplies
- Low power consumption:
  45 mW (600Ω 0 dBm load)
  30 mW (power amps disabled)
- Power down mode: 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

Block and Connection Diagrams

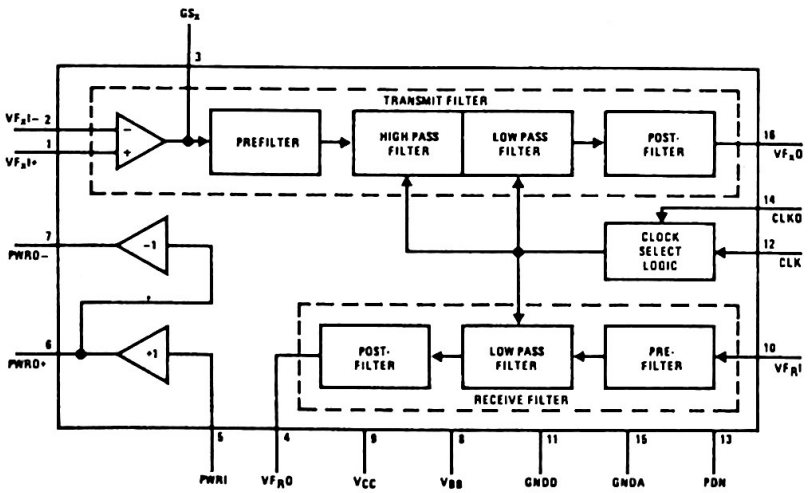
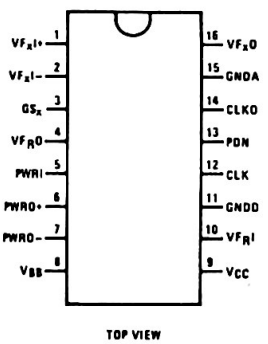


FIGURE 1

Dual-In-Line Package



TOP VIEW

IM-B25M121/Printed in U.S.A.

National Semiconductor

December 1981

TP50981/TP50981A, TP50982/TP50982A, TP50985/TP50985A Push Button Pulse Dialer Circuits

General Description

This family of monolithic CMOS circuits provides all logic necessary to convert keyboard inputs into a series of pulses simulating rotary telephone dialing. An on-chip memory capable of storing up to 17 digits allows keyboard entries to be made at rates comparable to those of tone-dialing telephones and provides one-key redial of the last number dialed. The keyboard inputs interface directly to a standard 2-of-7 keypad with positive-common or an inexpensive form A-type keyboard. Two outputs, one for pulsing the telephone line and one to mute the receiver, are provided along with pin selectable Break/Make ratios and an on-chip voltage regulator. The low voltage and low current requirements of these devices allow direct telephone line powered operation.

Features

- TP50981/TP50981A, TP50985/TP50985A for pulsing loop in shunt with speech network
- TP50982/TP50982A for pulsing loop in series with speech network
- 1.7V, 150 μA operation TP50981A, TP50982A and TP50985A
- Single-contact or positive-common key inputs
- Break/Make ratio pin selectable
- On-chip voltage regulator
- On-chip oscillator using 480 kHz ceramic resonator
- Scratchpad (new number storage without dialing) on TP50985/TP50985A
- 10/20 pps option on TP50985/TP50985A

Block Diagram

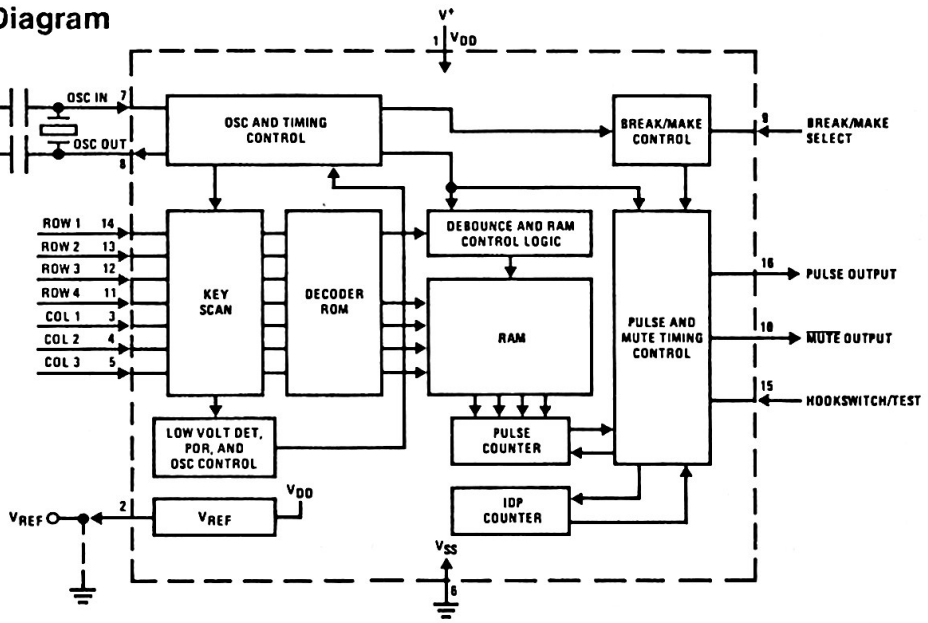
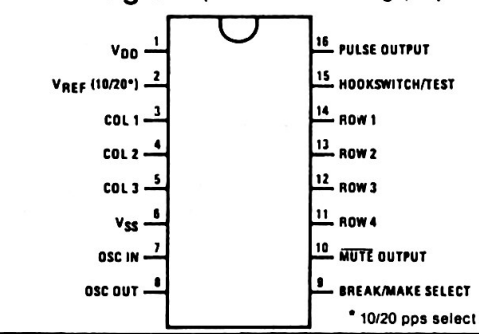


FIGURE 1

Connection Diagram (Dual-In-Line Package, Top View)



* 10/20 pps select input on TP50985/TP50985A

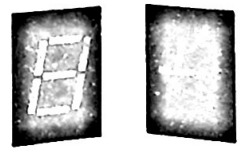
Order Number TP50981N, TP50981AN, TP50982N, TP50982AN, TP50985N or TP50985AN

IM-B25M121/Printed in U.S.A.

National Semiconductor

November 1981

5082 Series 0.43 Inch 7-Segment and Overflow Displays



5082-7650 Series High Efficiency Red
5082-7660 Series Yellow
5082-7670 Series Green
5082-7750/-7760 Series Standard Red

General Description

The 5082-7650/-7660/-7670/-7750/-7760 series are large 0.43 inch (10.92 mm) LED 7-segment displays. Designed for viewing distances up to 6 meters (19.7 feet), these single digit displays provide a high contrast ratio and a wide viewing angle.

These devices utilize a standard 0.3 inch (7.62 mm) dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets.

The 5082-7650 and 5082-7660 series devices utilize high efficiency LED chips which are made from GaAsP on a transparent GaP substrate. The 5082-7670 series devices utilize chips made from GaP on a transparent GaP substrate. The 5082-7750/-7760 series uses standard red GaAsP on GaAs substrate.

Absolute Maximum Ratings (25°C)

Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +85°C
Peak Forward Current per Segment or DP	60 mA
DC Forward Current per Segment or DP	20 mA
Lead Soldering Temperature [1/16 inch (1.59 mm) Below Seating Plane]	260°C for 3 Sec

Devices

Part Number	Color	Description	Internal Circuit Diagram
5082-7650	High Efficiency Red	Common Anode Left Hand Decimal	A
5082-7651	High Efficiency Red	Common Anode Right Hand Decimal	B
5082-7653	High Efficiency Red	Common Cathode Right Hand Decimal	C
5082-7656	High Efficiency Red	Universal Overflow ±1 Right Hand Decimal	D
5082-7660	Yellow	Common Anode Left Hand Decimal	A
5082-7661	Yellow	Common Anode Right Hand Decimal	B
5082-7663	Yellow	Common Cathode Right Hand Decimal	C
5082-7666	Yellow	Universal Overflow ±1 Right Hand Decimal	D
5082-7670	Green	Common Anode Left Hand Decimal	A
5082-7671	Green	Common Anode Right Hand Decimal	B
5082-7673	Green	Common Cathode Right Hand Decimal	C
5082-7676	Green	Universal Overflow ±1 Right Hand Decimal	D
5082-7750	Red	Common Anode Left Hand Decimal	A
5082-7751	Red	Common Anode Right Hand Decimal	B
5082-7756	Red	Universal Overflow ±1 Right Hand Decimal	D
5082-7760	Red	Common Cathode Right Hand Decimal	C

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See Internal Diagram.

IM-B25M111/Printed in U.S.A.

THE DATA BOOKSHELF: TOOLS FOR THE DESIGN ENGINEER

National Semiconductor's Data Bookshelf is a compendium of information about a product line unmatched in its breadth in the industry. The fifteen independent volumes that comprise the Bookshelf—about 8000 pages—describe in excess of 8100 solid-state devices; devices that span the entire spectrum of semiconductor processes, and that range from the simplest of discrete transistors to microprocessors—those most-sophisticated marvels of modern integrated-circuit technology.

Active and passive devices and circuits; hybrid and monolithic structures; discrete and integrated components...complete electrical and mechanical specifications; charts, graphs, and tables; test circuits and waveforms; design and application information...whatever you need, you'll find it in the designer's ultimate reference source—National Semiconductor's Data Bookshelf.

AUDIO/RADIO HANDBOOK

This 240 page handbook acquaints those involved in audio systems design with National Semiconductor's broad selection of integrated circuits specifically designed for accurate audio reproduction.

Far from just a collection of data sheets, this manual contains detailed discussions, including complete design particulars, covering many areas of audio.

Thorough explanations, complete with real-world design examples make clear several audio areas never before available to the general public.

Page Count: 240 Price: $5.00 Year: 1980

CMOS DATA BOOK

This databook contains information on National Semiconductor's standard SSI/MSI CMOS products. This includes the popular 54C74C series logic family, which is pin for pin, function for function equivalent to the 7400 family of TTL devices. All device outputs are LPTTL compatible, capable of sinking more than 360μA ($\approx$ 1 LSTTL load). The AC parameters are specified with a 50pF capacitive load.

In addition, this book describes National Semiconductor's extensive line of CD40XXB and CD45XXB series devices. These parts meet the standard JEDEC "B-Series" specifications.

Special Function, LSI, A/D Converters and Memory device specifications contained herein offer the designer unique high density low power system solutions. All devices are compatible with 54C/74C series and CD4XXB series products.

Page Count: 842 Price: $6.00 Year 1981

DATA CONVERSION/ACQUISITION DATABOOK

National Semiconductor provides 864 pages of in-depth component and application data about devices in the direct analog signal path before (and after) the digital processor.

With high volume production capabilities, National Semiconductor has become a leader in data conversion/acquisition by utilizing state of the art processes like BI-FET™, linear bipolar, CMOS, thin film, laser trimming, I^2L, and hybrid.

Selection guides for analog switches/multiplexers, A/D and D/A converters, sample and hold, and voltage reference, and a data conversion/acquisition circuits cross reference guide, along with an alphanumeric index, facilitate quick and easy information selection.

Page Count: 864 Price $7.00 Yer: 1980

48-SERIES MICROCOMPUTER HANDBOOK

This handbook contains detailed design-related information pertaining to the National Semiconductor 48-Series single-chip microcomputers and microprocessors.

The material presented is at a level of detail to aid in the design and development of systems using the 48-series microcomputers.

Topics include the 48-series architecture, expansion, and instruction set.

Additional hardware examples, integrated with the required software, and various data sheets of compatible devices are given.

Page Count: 192 Price: $5.00 Year: 1980

HYBRID PRODUCTS DATABOOK

The Hybrid Products Databook is the only National Semiconductor publication that contains complete information on all of our hybrid semiconductor products.

Included are precision thin film and thick film products which provide the user with standard functions from operational amplifiers to converters with capabilities beyond those of current monolithic technology.

Product selection guides and an application section are also included.

Page Count: 792 Price: $7.00 Year: 1982

THE INTERFACE DATABOOK

In National Semiconductor's Interface Databook, 702 pages of specifications describe one of the industry's broadest lines of interface products.

Over 300 data sheets have been compiled, covering transmission line drivers/receivers, bus transceivers, peripheral/power drivers, level translators/buffers, display drivers, MOS and magnetic memory interface circuits, microprocessor support circuits, applicable TTL and CMOS logic circuits.

An industry cross reference guide gives National Semiconductor's exact replacement for 7 other manufacturers. Product selection guides and a complete product applications section make it easy to find the correct part number for these specialized ICs.

Page Count: 702 Price: $6.00 Year: 1980

LINEAR APPLICATIONS HANDBOOK

This 712 page handbook provides a fully indexed and cross referenced collection of 110 linear circuit applications using both monolithic and hybrid circuits from National Semiconductor's broad line of linear products.

Through provoking applications, written by National's engineers, are an excellent reference source for linear design problems.

Consumer applications; frequency, temperature and drift compensation; and improving signal to noise ratios are just a few of the design requirements considered.

Page Count: 712 Price $16.00 Year: 1980

LINEAR DATABOOK

The 1980 Linear Databook provides over 1,300 pages of up-to-date information about National's broad line of linear components.

Selection guides, term definitions, features, and diagrams are included for voltage and precision regulators, op amps and instrumentation amplifiers, analog switches/multiplexers, sample and hold, A/D and D/A converters, audio, radio and TV circuits, and transistor/diode arrays.

A usage breakdown is given for components in various industrial, automotive, appliance, functional blocks and telecommunications applications.

Appendices include extended quality and reliability programs, MIL-STD-883/MIL-M-38510 information, and linear and industry cross reference guides.

Page Count: 1376 Price: $9.00 Year: 1980

LOGIC DATABOOK

National's new Logic Databook covers five of their logic families: TTL (54/74), Schottky (54S/74S), low power Schottky (54S/74LS), high speed (54H/74H), and low power (54L/74L).

The Logic Databook—specially organized for quick and easy referencing—offers two complete functional indices and selection guides, one for SSI and one for MSI devices. In addition, it includes over 100 connection diagrams and test waveforms to help speed the design-in cycle.

All in all, it's probably the most comprehensive collection of practical information ever assembled on such a broad line of practical components.

Page Count: 624 Price: $9.00 Year: 1981

MEMORY DATABOOK

National Semiconductor has continued its reputation as a high volume supplier of high quality, cost-effective components by expanding into the design and processing of semiconductor memories.

While developing this state-of-the-art technology, National met the problems of industry standardization by proposing and utilizing new terminology and symbols to make all memory data sheets consistent. Hence, a cohesive, 464 page databook that includes selection guides, diagrams, and test characteristics for RAMs, EPROMs, MOS ROMs, and magnetic bubble memories.

Sections have also been devoted to character generators, memory support circuits, and physical dimensions.

Page Count: 464 Price: $6.00 Yea: 1980

NSC800 MICROPROCESSOR FAMILY HANDBOOK

Contained in this manual are 224 pages of design-related information about National Semiconductor's 800-family series of high-performance/low-power microprocessor components.

Included are hardware functions, software operations, system support and design considerations for the NSC800 CPU, the NSC810 RAM I/O Timer, and the NSC830 ROM I/O.

Completing this current edition are data sheets, application notes, and physical dimensions for many of the NSC800 components fabricated using the P²CMOS process.

Page Count: 224 Price: $5.00 Year: 1981

PAL™ DATABOOK

This book is intended to be a complete reference for the design of digital systems using Programmable Array Logic (PAL) devices. In addition to data sheets for all currently available devices, this book also contains extensive application notes intended to give design examples for a number of PAL devices. It also contains a step-by-step procedure for PAL design and programming, including the listing for PALASM™ which is a FORTRAN IV program that converts logic equations to PAL programming information.

Portions of this book have been reprinted with the permission of Monolithic Memories Inc., the originator of the PAL concept.

Page Count: 176 Price: $6.00 Year: 1982

RELIABILITY HANDBOOK

This 832 page text is addressed not only to reliability specialists, but to designers, specifiers, program managers, and procurement specialists to whom semiconductor reliability is of vital concern.

The first section is a general overview of semiconductor devices, examining tests that include electrical, mechanical, environmental, and visual tests.

Thoroughly explained are the 883B and 883S RETS™ requirements and their relationship with linear, hybrid, interface, data acquisition, microprocessor and memory, CMOS and bipolar logic high reliability microcuits made by National Semiconductor.

The handbook is voluminously documented and comprehensively cross referenced.

Page Count: 832 Price: $20.00 Year: 1979

SERIES/80 BOARD LEVEL COMPUTER STARPLEX™ DEVELOPMENT SYSTEM DATABOOK

This databook provides 224 pages of summary information on the complete line of SBC compatible board and system level microcomputer products, as well as information about the National Semiconductor Starplex™ development system.

Photos, product overviews, and specifications comprise over 50 BLC and RMC data sheets presented.

The Starplex Development System section is user-oriented. Featured are the disc operating system, FORTRAN IV and BASIC, the text editor, and options like the IN-SYSTEM EMULATOR™ and Starlink™. CPU instructions and National Semiconductor training courses conclude the databook.

Page Count: 224 Price: $5.00 Year: 1980

VOLTAGE REGULATOR HANDBOOK

With the variety of fixed and variable regulator technology currently available, the 336 page Voltage Regulator Handbook becomes a must for the selection of three-terminal and dual tracking components that meet the system requirement while utilizing the most cost-effective approach.

Beginning with product selection procedure and a data sheet summary, the text continues with easily accessible information about booster circuitry, power transformer and filter specifications, test methods, manufacturers' cross reference, and extended use applications for National's regulators.

Page Count: 336 Price: $7.00 Year: 1982

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